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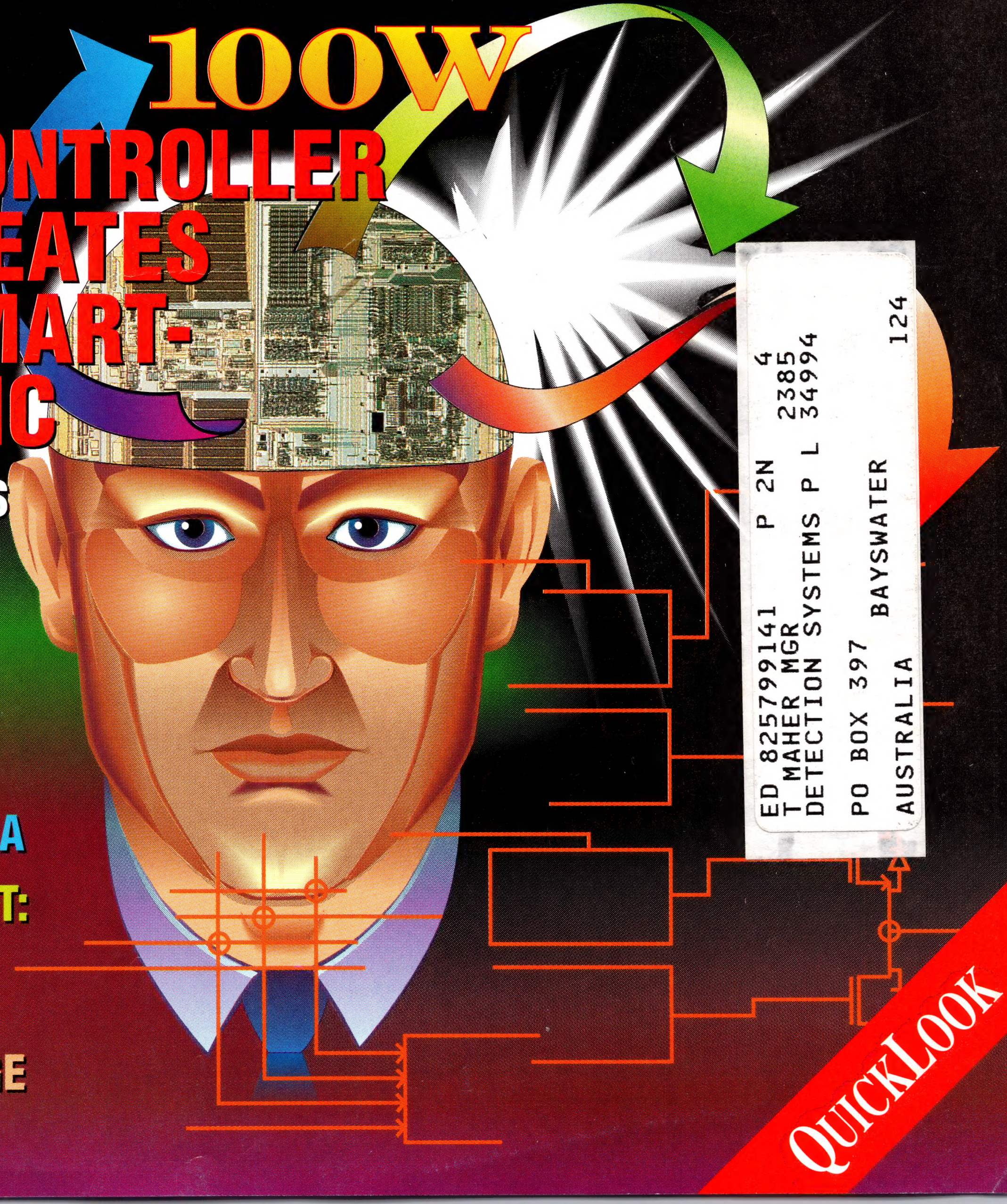

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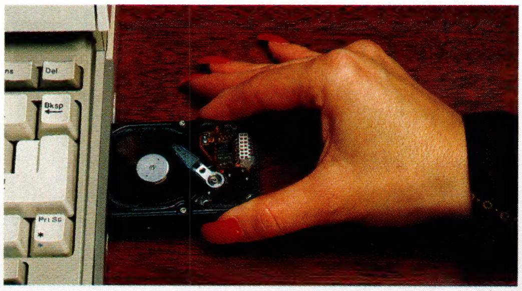

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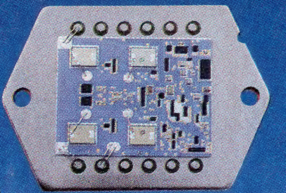

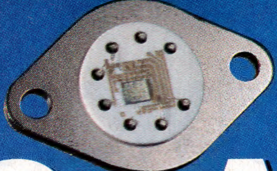

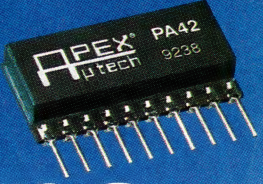

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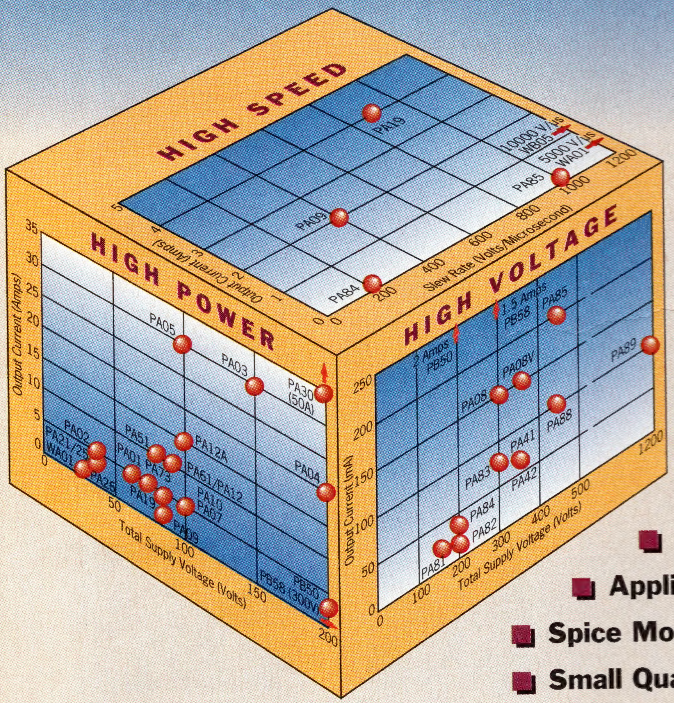

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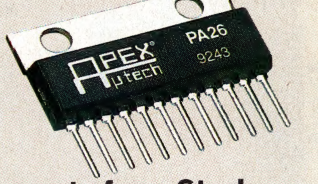

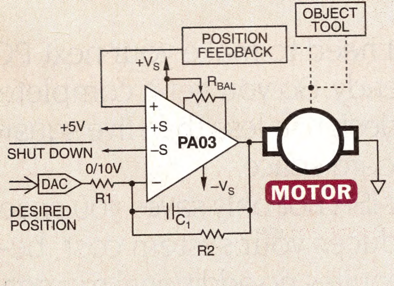

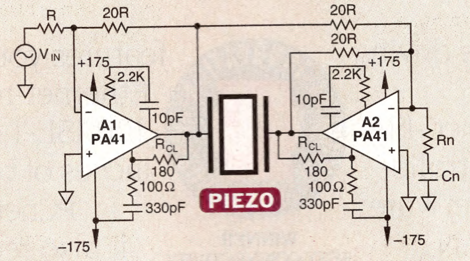

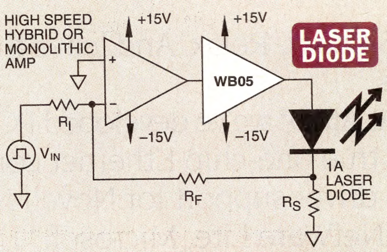

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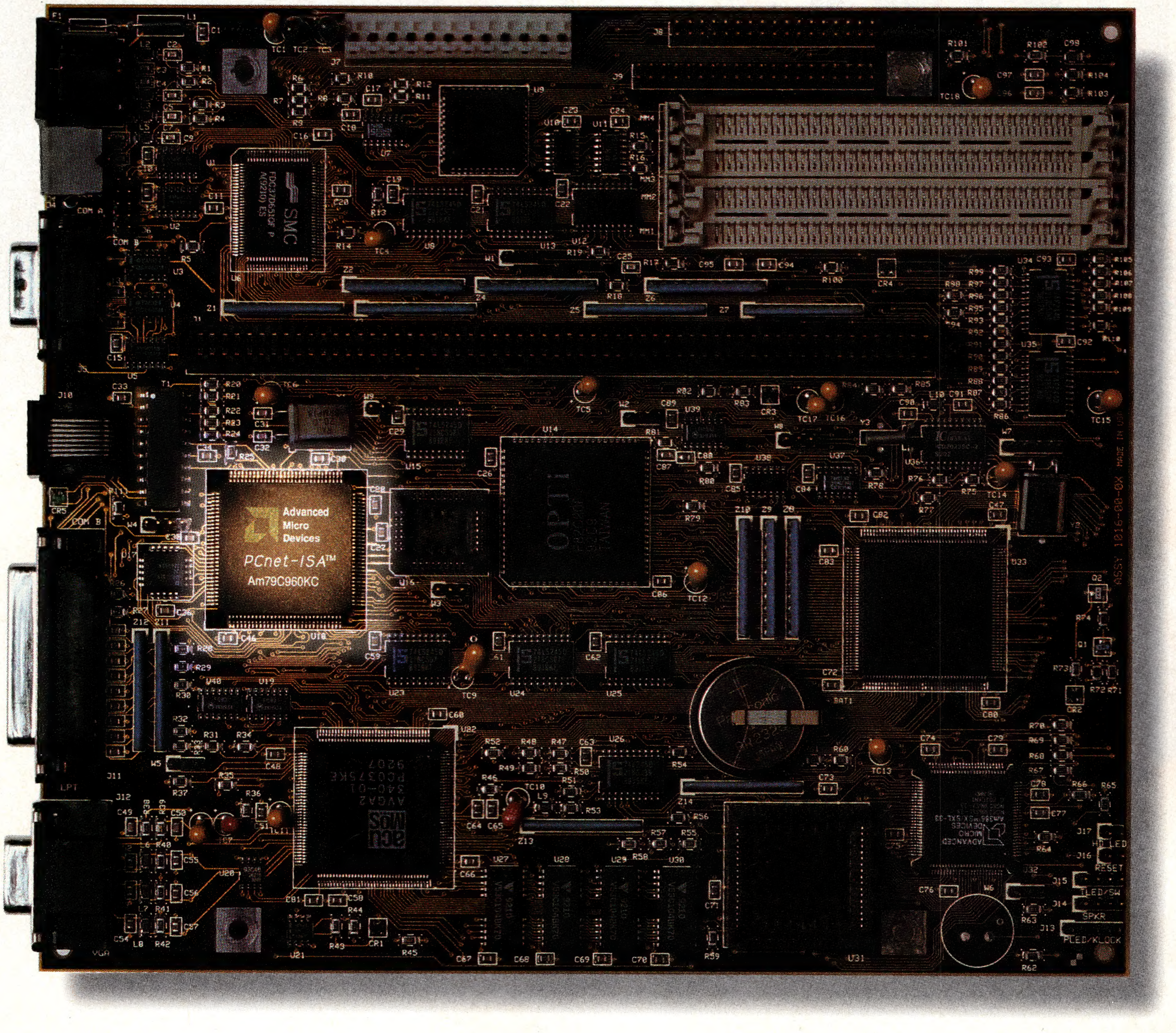

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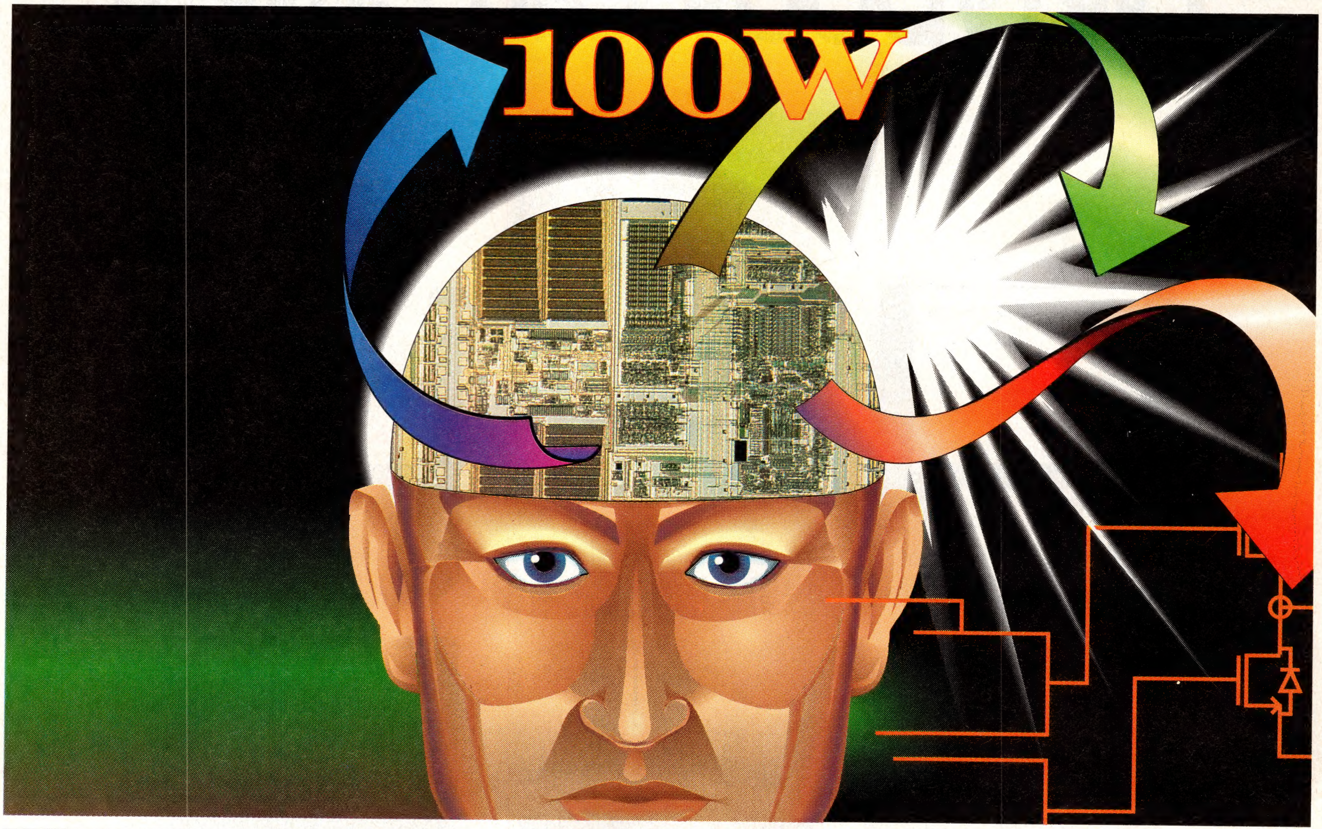

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ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published semi monthly except for 3 issues in May and 3 issues in November by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $95 U.S., $175 Canada, $255 International. Second-class postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204.

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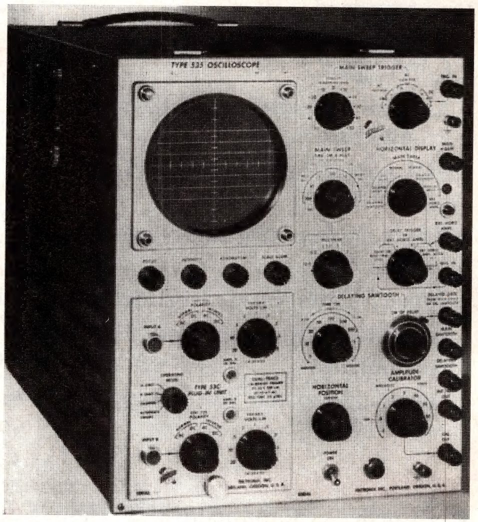
ELECTRONIC DESIGN 40 YEARS AGO

Cathode-Ray Oscilloscope With Plug-In Preamplifiers

Providing the Type 535 Cathode-Ray Oscilloscope with plug-in preamplifiers has resulted in a versatile instrument capable of covering the complete range of facilities which formerly required the use of three or more separate high quality laboratory scopes. The unit (shown), also has a new accurate sweep delay circuit, a wide time-base range, and high accelerating potential, making it adaptable to almost any phase of laboratory development investigation.

The sweep circuit provides 24 calibrated sweeps from 0.1msec/cm to 5sec/cm with accurate 5x magnification on all ranges, and continuously variable uncalibrated sweeps from 0.1msec/cm to 10sec/cm. Automatic main sweep lockout with controllable reset permits accurate delay of the start of the main sweep from 10msec to 20,000msec. A 10kv accelerating potential is provided for the Type 51P2 metallized 5" cathode-ray tube, and the square-wave amplitude calibrator covers a range of 0.2mv to 100v.

Three different plug-in preamplifiers are available for use with the instrument, which is a product of Tektronix, Inc. (P.O. Box 831, Portland 7, Ore.) Additional plug-in units are being developed.



The Type 53C Dual Trace Unit has two identical amplifier channels, activated on alternate sweeps, or nonsynchronously, at about 100kc. Both channels have a 0.04msec rise time, d-c to 8.5Mc bandpass, and 0.05v/cm to 20v/cm sensitivity in nine calibrated steps. Sensitivity is continuously variable between steps and extends to 50v/cm. A four-position a-d/d-c and polarity reversal switch is provided for each channel.

The Type 53D Differential High Gain d-c Unit has a sensitivity of 1 mv/cm to 50v/cm in 24 calibrated steps, with variable sensitivity between steps. Band-pass is d-c to 250kc at maximum sensitivity, extending to 750kc at 50mv and lower. A six-position a-d/d-c input selector switch is provided. The Type 53A Wide-Band d-c Unit has a 0.035msec rise time, d-c to 10Mc bandpass, and 0.5v/cm to 20v/cm sensitivity in nine calibrated steps. Sensitivity is continuously variable between steps and extends to 50v/cm. Two signal inputs with 60db isolation are provided, as well as a four-position a-c/d-c and input selector switch.

Waveforms available from the front panel include positive gate, delayed gate, main sawtooth, internal trigger, and a calibrating square wave. The instrument also has a beam position indicator in which indicator lights show the location of the cathode-ray electron beam when it is off the screen. The horizontal input amplifier has a sensitivity of 0.2v/cm to 20v/cm which is continuously variable. Direct-coupled unblanking assures a constant unblanking level when changing sweep rates and duty cycle. A new balanced delay network (0.25msec signal delay) to provide superior transient response and a 50cy to 50kc repetition rate source are other features. (*Electronic Design, October 1953, p. 12.*)

The 530 series plug-in oscilloscopes demonstrated the market savvy and technical expertise of Tektronix founder Howard Vollum. The scopes also led to a management crisis within the young company, according to the company history Winning With People: The First 40 Years of Tektronix. *Vollum wanted to offer users the versatility of a plug-in scope, while Tek partner Logan Belleville wanted to a separate scope for each specific purpose. Belleville, a former member of the WWII MIT Radiation Lab staff, ended up leaving the company in late 1953, while Vollum served as Tektronix's leader until retiring in 1983.—Ed.*

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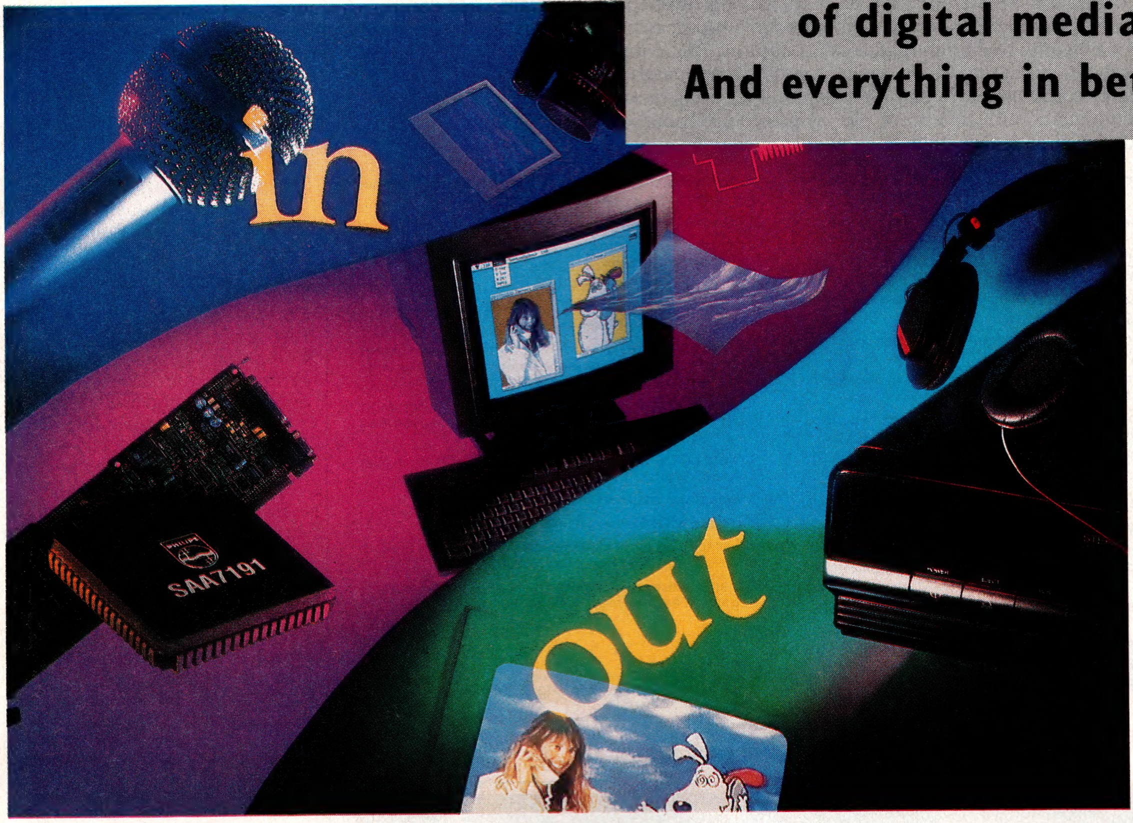

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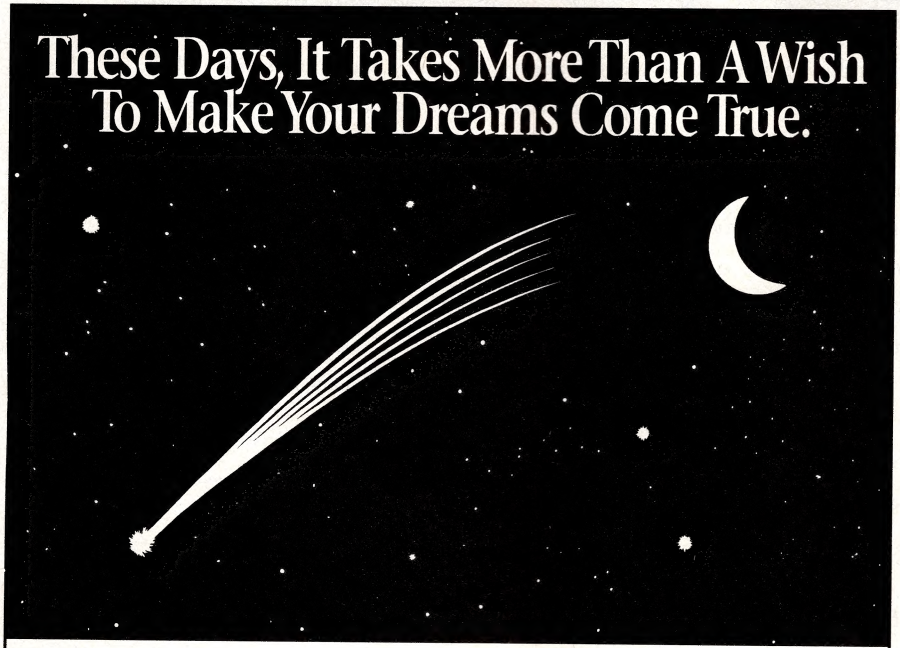

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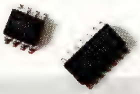

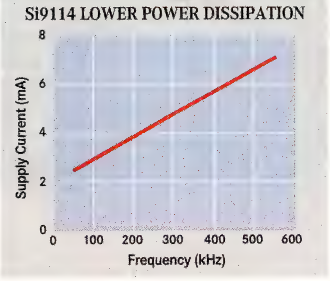

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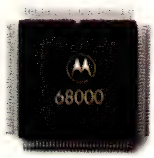

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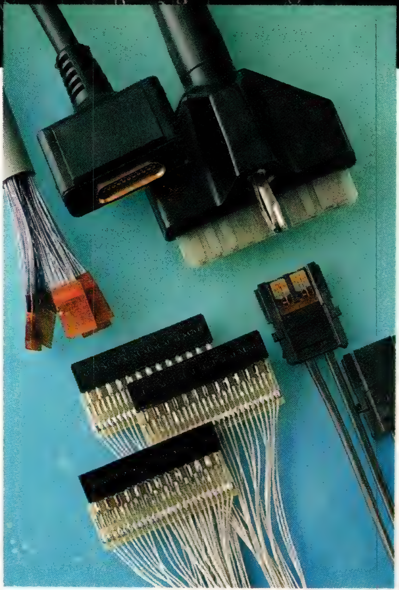

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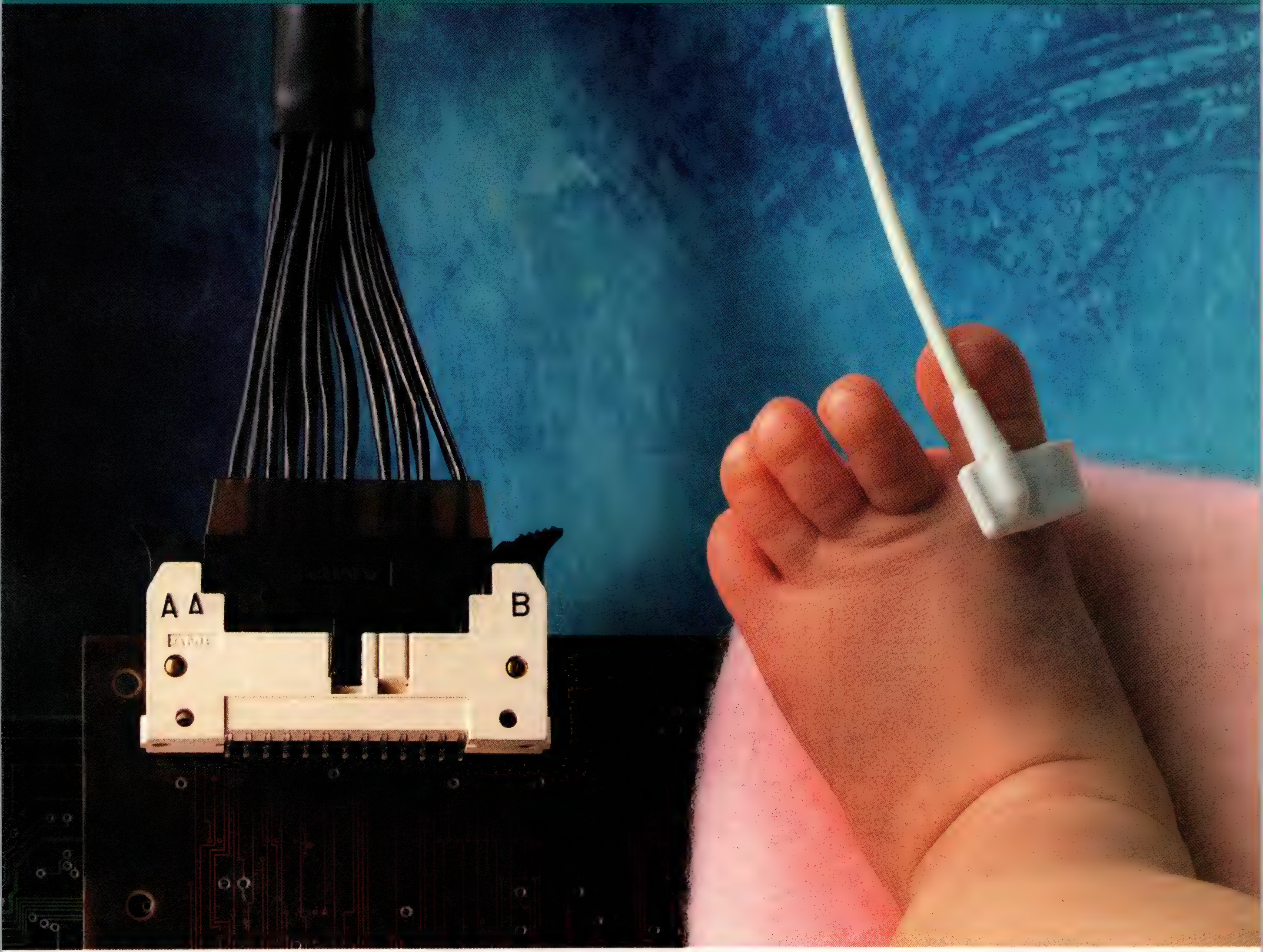

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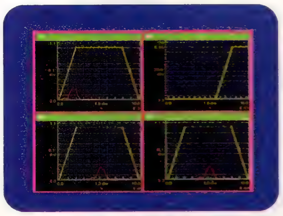

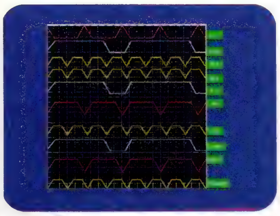

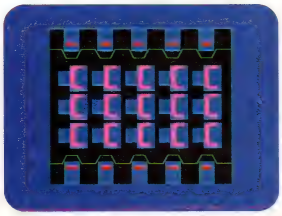

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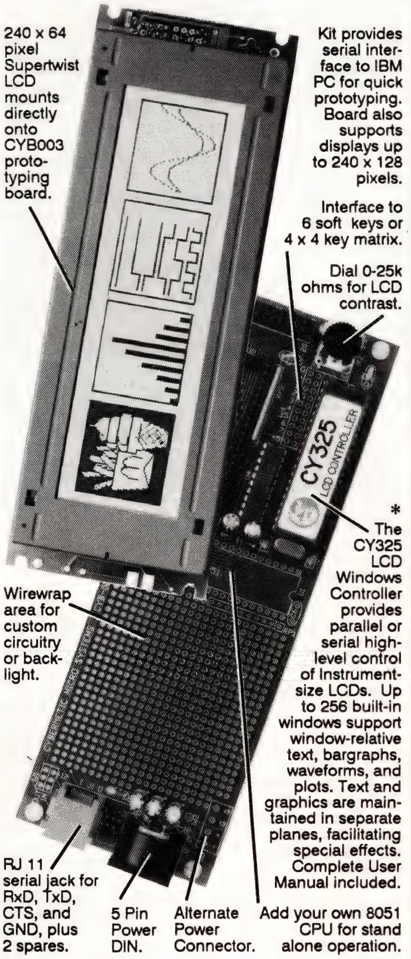
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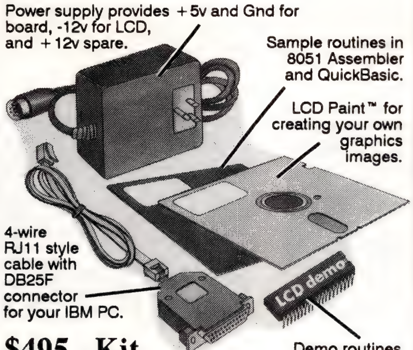
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CIRCLE 104 FOR U.S. RESPONSE
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RETOOLING THE INFRASTRUCTURE

The Federal Communications Commission finally took action on giving RF-spectrum space to new wireless communications services by reallocating frequencies in three bands—1850 to 1970, 2130 to 2150, and 2180 to 2200 MHz. In addition, they plan to start auctioning off operating licenses next year (which the Government hopes will add about $10 billion to its coffers). What impact will this have on the industry? Simply, it removes a major roadblock in the path to a large market for new devices and equipment. It also highlights an interesting reversal of trends in two basic communications systems—television and voice/data communications—and the problems of changing infrastructures when major technology changes occur.

In the old days, telephones were hardwired and television entered the home through the air from a single transmitting antenna. Today, in television, we are seeing over-the-air transmissions being superseded by cable hookups carrying many more TV channels as well as extra facilities offered by broadband media—interactive television, utility meter reading, etc. The wired connection seems appropriate here because television, as primarily an entertainment medium, involves static usage (witness the well-known couch potato), and the other services likewise will be directly related to the home.

However, in voice and data communications, the trend has flipped in the opposite direction, away from the wire tether in the home and office to a wireless system where signals interact with multiple antennas. This type of communications is becoming an increasingly integral part of today's mobile society. With the new personal communications services, the intelligent network will route calls to wherever that particular person happens to be.

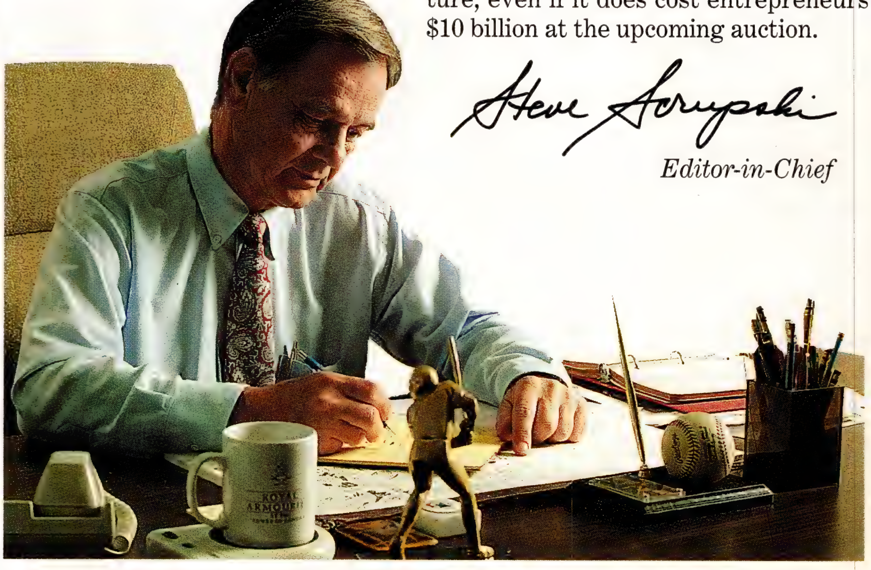
What becomes apparent here is that when a technology is young, its customers must adapt to it and accept its limitations. However, when the technology advances to a certain point, it can be configured within an infrastructure that adapts to the customers' needs and greatly expands the system's resources.

Changes to an infrastructure are difficult to achieve, though, when numerous companies over many years have made large investments in the previous structure. Three groups with wires entering the home—cable-TV, telephone, and utility companies—now are competing for the lead position in delivering on the promise of a broadband connection to the home. In wireless communications, telephone companies and cellular-system owners will soon be joined by many new wireless-services companies.

Unfortunately, what it appears to come down to is that the Government must play a role in reshaping the infrastructure, even if it does cost entrepreneurs $10 billion at the upcoming auction.

Steve Scrupski

Editor-in-Chief



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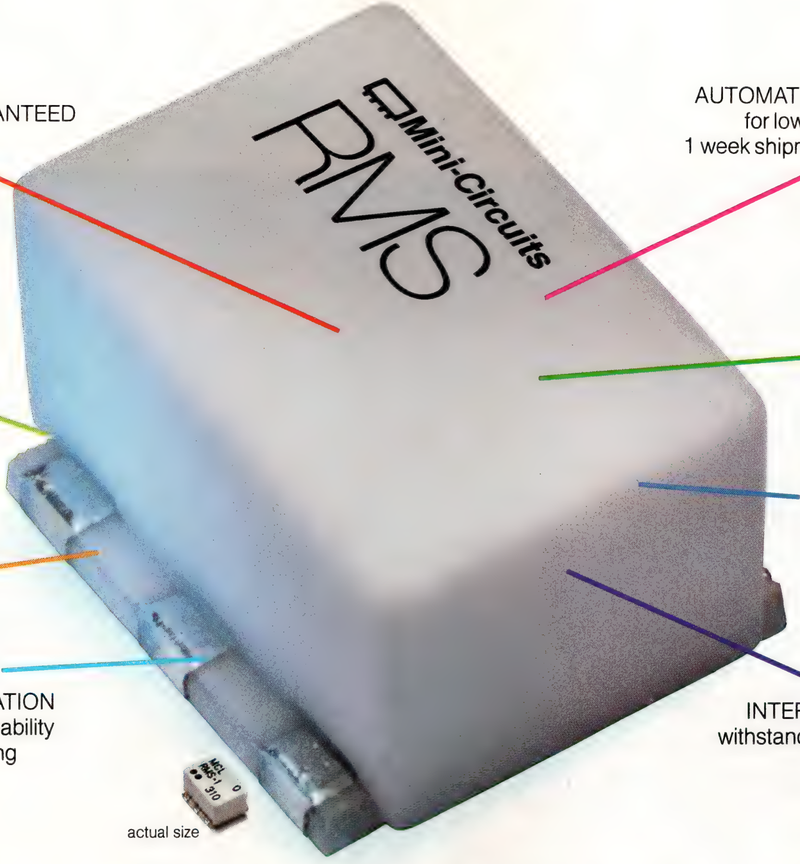

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	KM684002	512K x 8	15/20/25	SOJ(R)	'93,2Q	
	KM6164002	256K x 16	20/25	SOJ(R)	'93,3Q	
	KM64V4002	1M x 4	20/25	SOJ(R)	'93,2Q	3.3V
	KM68V4002	512K x 8	20/25	SOJ(R)	'93,2Q	3.3V
	KM616V4002	256K x 16	25	SOJ(R)	'93,3Q	3.3V
1M	KM64B1003	256K x 4	10/12	SOJ(R)	NOW	BiCMOS
	KM68B1002	128K x 8	10/12	SOJ(R)	NOW	BiCMOS
	KM641003	256K x 4	15	SOJ(R)	NOW	
	KM681002	128K x 8	15	SOJ(R)	NOW	
	KM6161002	64K x 16	15	SOJ(R)	NOW	
	KM64V1003	256K x 4	15	SOJ(R)	'93,3Q	3.3V
	KM68V1002	128K x 8	15	SOJ(R)	'93,3Q	3.3V
	KM616V1002	64K x 16	15	SOJ(R)	'93,3Q	3.3V
	KM741006	256K x 4	10/12.5	SOJ(R)	NOW	Syn.

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	KM684000-V	512K x 8	75/85/100	DIP/SOP/TSOP	NOW	3.3V
	KM658512	512K x 8	80/100	SOP/TSOP	NOW	Pseudo
1M	KM681000	128K x 8	70/85/100	DIP/SOP/TSOP	NOW	
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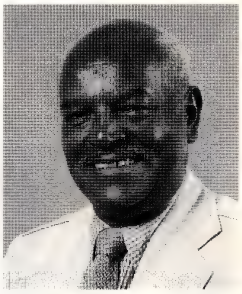
CIRCLE 238 FOR U.S. RESPONSE
CIRCLE 239 FOR RESPONSE OUTSIDE THE U.S.

WIRELESS STANDARDS ARE LONG OVERDUE

The flood of incompatible wireless-LAN (WLAN) products pouring into the industry has reached the crisis stage for both end users and information-service managers, and could very well delay the anticipated quick upward turn in the market. "The wireless LAN industry is at a crossroads. It can continue to plod along without standards, or get into a hockey-stick-like growth with open standards," according to Richard Siber, director of the Mobile Communications Group at BIS Strategic Decisions. Without standards, many users are worried about betting on the wrong horse, much like the Betamax/VHS scenario.

The proliferation of incompatible WLAN platforms will also impact software development. Only when standards are developed to define how WLAN nodes behave will developers of network operating systems and ad-hoc networking applications be able to propagate the enabling software, such as drivers and integrated network management, that's needed to fuel the mass market. Toward this end, the IEEE 802.11 WLAN committee is trying to create a unified Media Access Control (MAC) standard that will foster interoperability between WLAN equipment from various vendors. The MAC protocol implements the lower half of Layer 2 of the OSI (Open Systems Interconnection) reference model that governs access to the transmission media.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However, the challenge for any standards committee is to balance the need for a satisfactory technical solution against the pressure from early market entrants who promote proprietary systems. "Open standards for WLANs should be based on technological excellence and the need to quickly complete a minimum subset of standards to ensure that WLANs from different vendors will interoperate," says Gary Johnson, director of the wireless networking business group at National Semiconductor Corp., Santa Clara, Calif.

Since March of last year, the 802.11 committee has narrowed the field of contenders to three MAC protocol submissions. One is a reservation-based protocol that uses a central control point to schedule transmissions. The transmitting station waits for the contention time of the protocol's constant-length frame and transmits a short request-to-send (RTS) message to the point control function (CF). In the next frame, if the network is not too busy, the point CF notifies the station of its transmission time. Another contender is the Hybrid Carrier Sense, Multiple Access with Collision Avoidance (CSMA/CA) protocol. This is a listen-before-talk protocol that's based on a distributed control function. The hybrid, which is a version of the CSMA/CA protocol once used with wired Ethernet LANs, uses RTS and clear-to-send (CTS) messages to avoid collisions. These messages tell stations within the range of both the sending and receiving nodes that a data packet is about to be transmitted and to stay off the channel for a specific time period. These two protocols are incompatible, and it could take the committee a year or two to make a choice. To expedite the decision, a third protocol proposed by National Semiconductor, called the Unified MAC protocol, combines the major elements of the other two.

From the end user's point of view, the industry is in dire need of WLAN standards to eliminate the risks of using proprietary products, limited interoperability, and early product obsolescence. Once set, the standards will enable all mobile computing platforms, including PDAs, notebooks, laptops, and desktops, to communicate with one another using multiple client-server and peer-to-peer networking operating systems. When this hurdle is negotiated, the industry can then focus on integrated network-management issues.

(As is evident here, one other element of the industry that's also in dire need of some control is the generation of acronyms. But that's another story for another day.)

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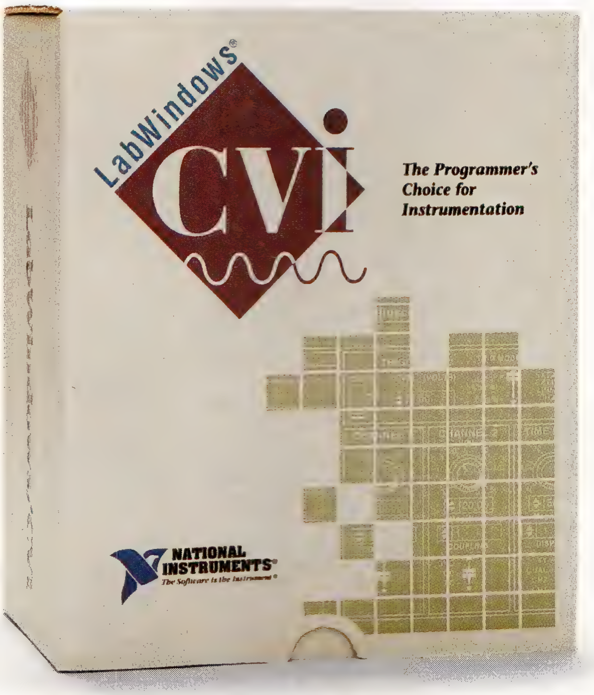
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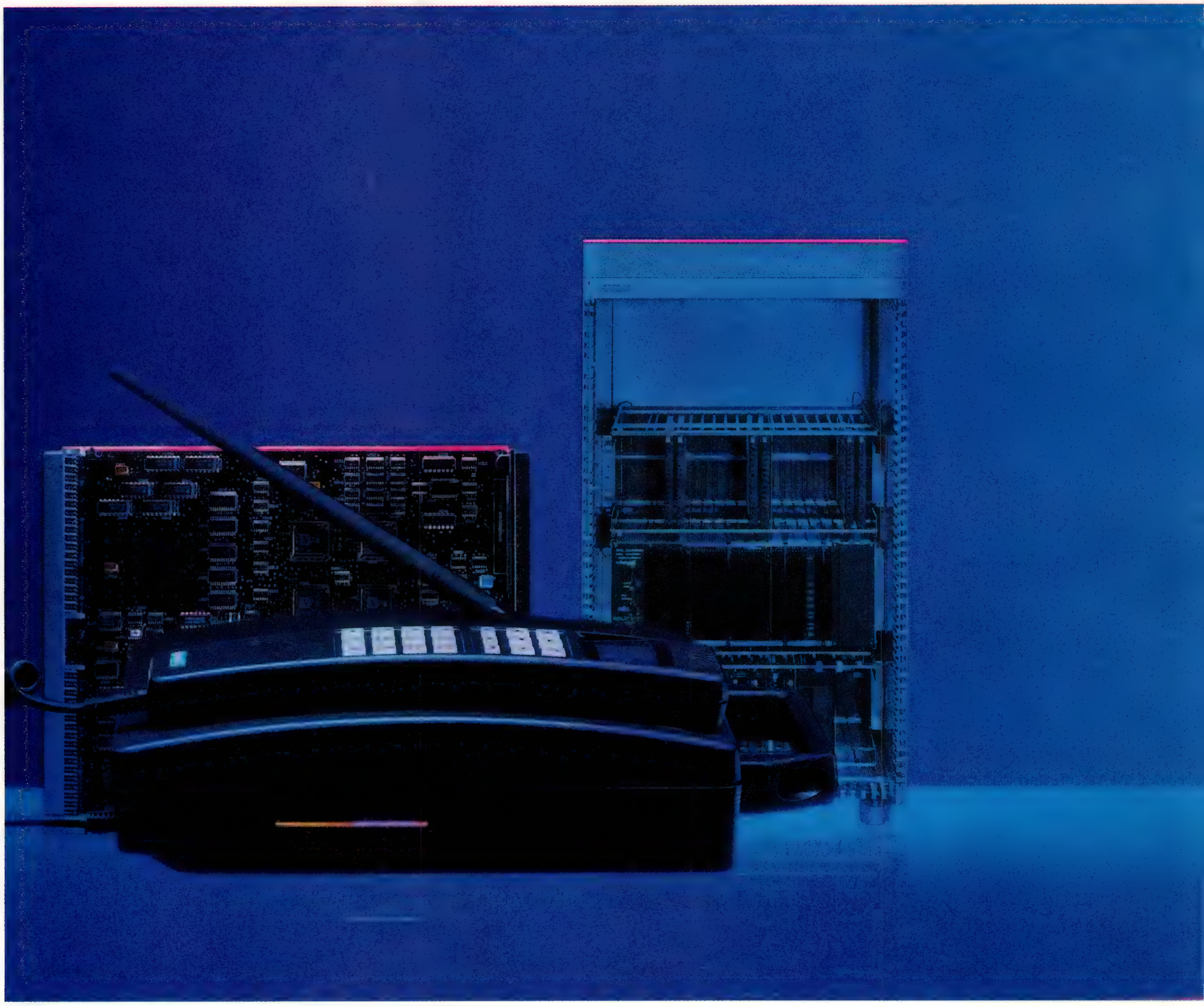

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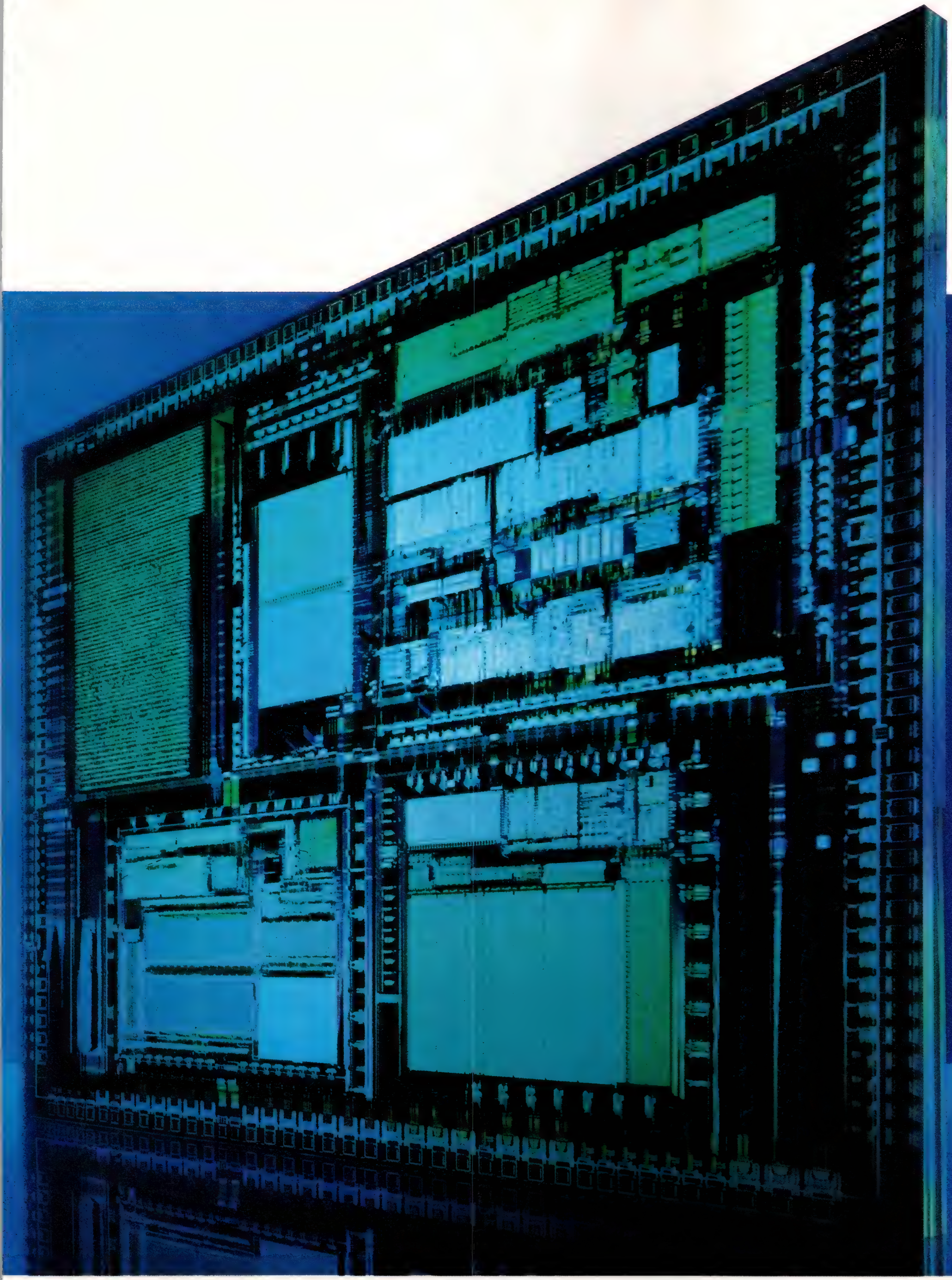

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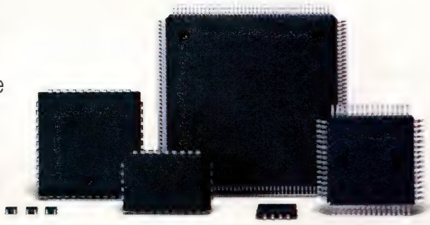

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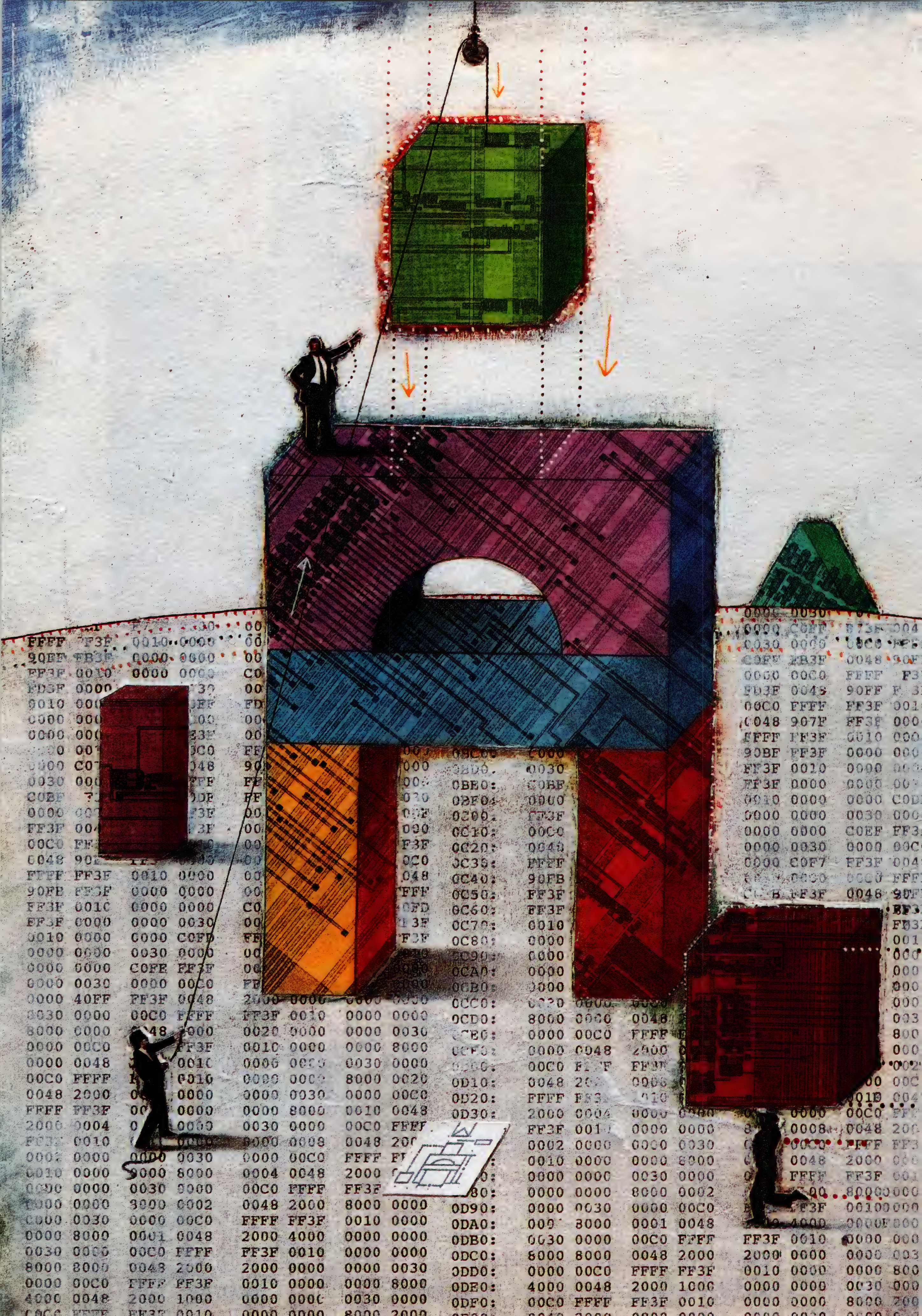

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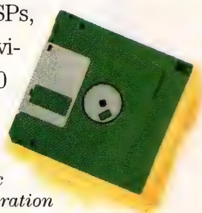

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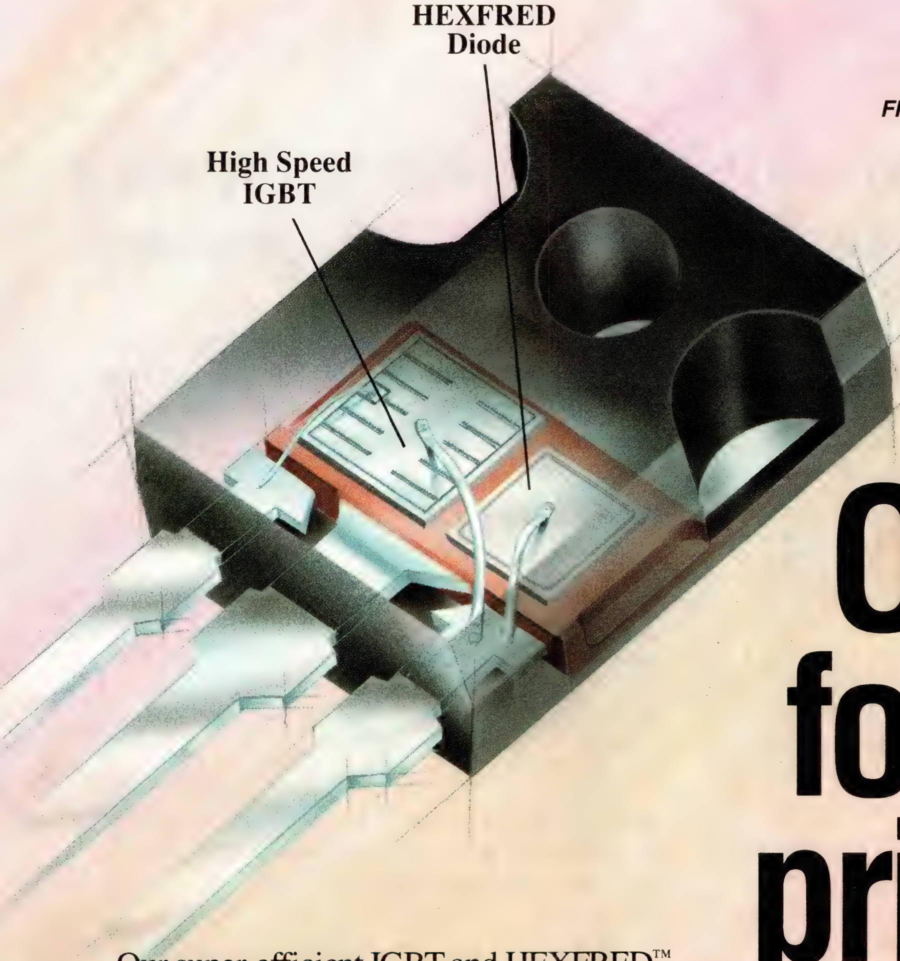

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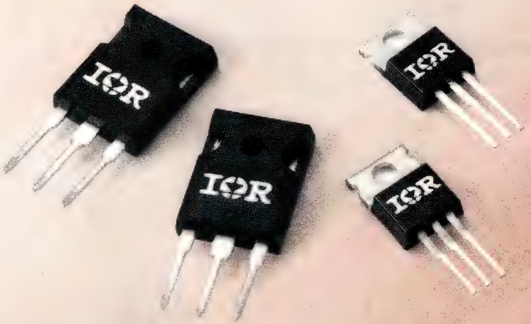

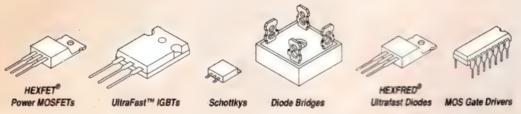

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TECHNOLOGY NEWSLETTER

PROPOSED AUDIO PROTOCOL MAY FOSTER A STANDARD

An audio protocol developed for a line of X terminals is under consideration by the X Consortium as an industry standard for playing, recording, and manipulating sound over a network. The Network Audio System protocol was submitted by Network Computing Devices Inc., Mountain View, Calif. The protocol supports multiple simultaneous applications and automatically handles format conversion among incompatible PCs, workstations, and X terminals. Applications specify how various inputs and outputs are hooked together, and the system automatically routes sound data to the proper destination. Sound may be stored in an audio server for replay, or streamed directly to output devices, such as speakers. The Network Audio System also permits dynamic volume adjustment and sound mixing. Network Computing Devices created a sample of the protocol's source code for the Sun OS 4.1 operating system, and is offering a free sample through the Internet network for public use and review. The consortium's main function is to develop and enhance the X-Window System. The Interactive Multimedia Association is an international trade group representing multimedia vendors and users. For more information, contact Network Computing Device's Judy Estrin at (415) 694-0650. ML

MOLDING MATERIAL AND PROCESS ISOLATE TO-220

An advanced molding compound and a new molding process were developed to fully isolate a TO-220 package with 2500 V rms of isolation, making it the first with such isolation for both single-clip and single-screw mounting. The package also has the equivalent thermal resistance of a 100-μm layer of insulating mica. Power devices built with the "Fullpak" packaging technique require no additional hardware or insulating material. Thus, they can be mounted directly to a conducting surface at a potential other than that of the device's internal pins. The new package, developed by International Rectifier, El Segundo, Calif., completely encloses the tab and drain with the new molding compound. The compound creates a thin layer over the tab to form a high-level electrical isolation layer. A special retracting-pin process during the molding step ensures a fully enclosed leadframe. The new technology also creates a more compact package, now just 10.5 mm wide by 16 mm high. The unique package design achieves a minimum creepage distance between pins of 2.65 mm and a minimum clearance of 4.8 mm—the best of any fully isolated TO-220 package. International Rectifier will eventually offer its complete TO-220 power-MOSFET line in the new package. Devices now offered in the package include a 16-V/14-A, 0.4-Ω FET; a 200-V/5.9-A, 0.4-Ω FET; and a 600-V/3.5-A, 1.2-Ω FET. For additional information, call Gene Sheridan at (310) 607-8978. FG

ALLIANCE GIVES TELECOMM DESIGNERS BETTER ACCESS

In a move that will give U. S. designers of telecommunications systems easier access to a wider array of test equipment, Tektronix Inc., Wilsonville, Ore., will now sell the RF and microwave communication and television test equipment developed by Rohde & Schwarz GmbH & Co. KG, Munich, Germany. Under a strategic alliance effective this month, Tektronix assumed exclusive marketing, distribution, service, and support responsibility for the Rohde & Schwarz products in the U. S. The German firm took on similar responsibilities for Tektronix's test and measurement products in Eastern Europe, most of the Mediterranean, the Middle East, and the Commonwealth of Independent States. The new agreement complements a move last June, when Tektronix agreed to distribute and service Advantest Corp.'s (Tokyo, Japan) RF, microwave, and communications products in the U. S., Canada, and Mexico. Rohde & Schwarz had already made such a pact with Advantest last year. JN

SCI SPECIFICATION NOW AVAILABLE FROM IEEE

The ANSI/IEEE standard 1596-1992, detailing the scalable coherent interface (SCI) specification, is now available. SCI offers users a single-chip interface that includes transceivers, FIFOs, and protocol logic. The interface supplies computer-bus-like services, yet delivers system performance higher than any bus can provide. That's due to a packet-based protocol, which is used over a large number of independent unidirectional point-to-point links. Initial links handle data rates of 1 Gbyte/s over a few meters, 1 Gbit/s over 20 meters using coaxial cable, or several kilometers using fiber optics. Interface chips are currently sampling. The published standard is easier to read and use than

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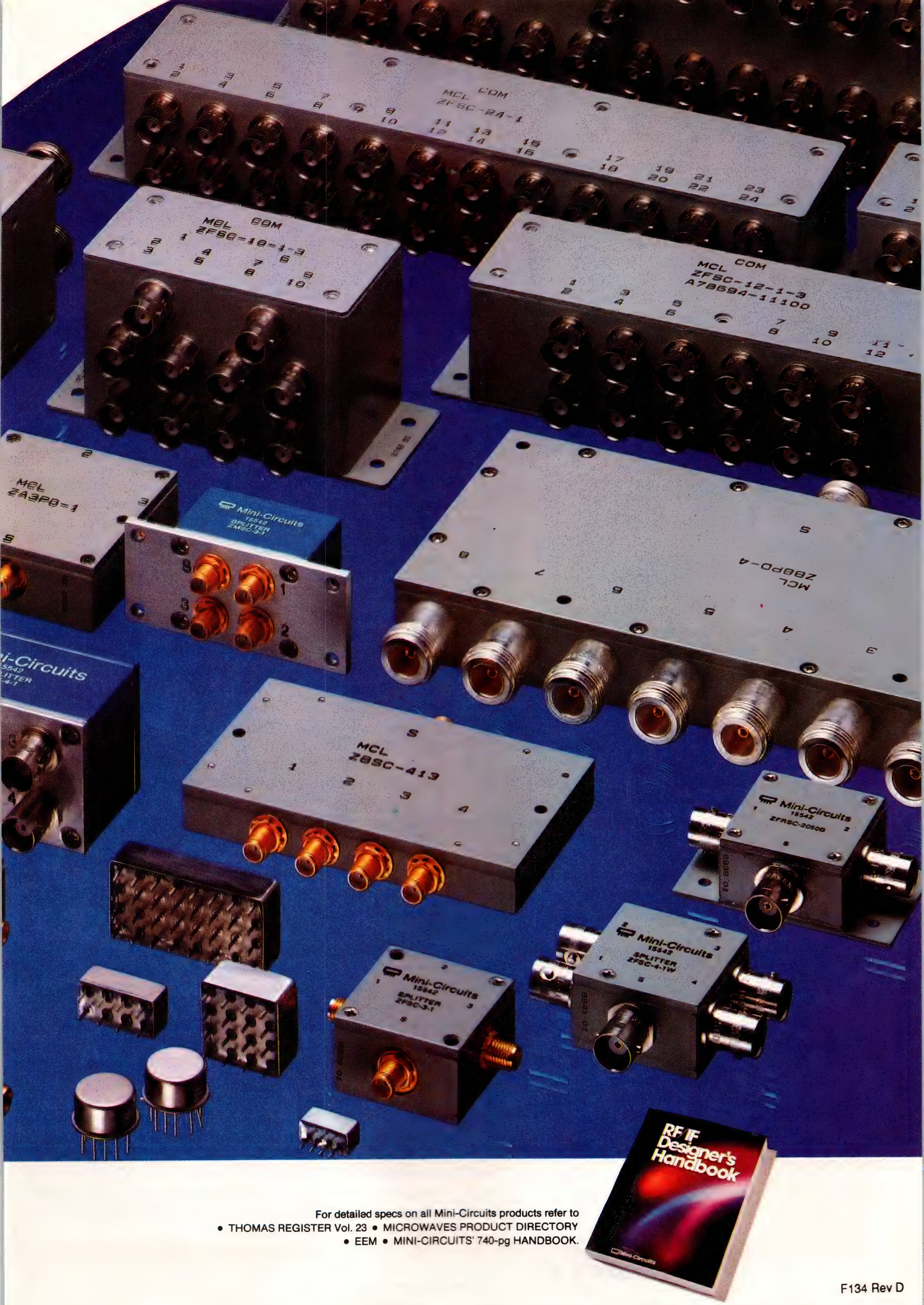

For detailed specs on all Mini-Circuits products refer to
• THOMAS REGISTER Vol. 23 • MICROWAVES PRODUCT DIRECTORY
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the draft document, mostly because the C-code listings are separate from the readable text. The executable C routines are shipped on a floppy disk. For more information, contact David Gustavson, 1596 working group chair, at (415) 961-3539. RN

V.FAST MODEM PROTOCOL HEADED FOR '94 APPROVAL

Study Group 14, the International Telecommunications Union group charged with developing a standard for higher-speed modem data transmission, has come up with a plan for approving the V.fast protocol by June of next year. In recognition of the new status given to the protocol, V.fast is now called Draft Recommendation V.34. "It would not be surprising to see V.34-compliant products on the market shortly after the finalized text is submitted to the ITU in February 1994," says Dick Brandt of AT&T and vice chairman of ITU-T Study Group 14. Brandt says that although some decisions on feature options are yet to be made, the sections dealing with the data mode are essentially complete. The group has now switched its focus to the startup section. By December of this year, the specification is expected to be completed. That will allow for some interoperability testing prior to putting the final text in the hands of the ITU Telecommunications Standardization Bureau by late February 1994. Brandt is optimistic that Recommendation V.34 will be approved by the Study Group in June 1994. For more information on the modem protocol, call AT&T's Dick Brandt at (908) 735-6171. ML

POWERPC HITS THE STREET RUNNING

The efforts of a joint development between Apple Computer, IBM, and Motorola, are starting to bear fruit: Four workstation and server platforms based on the PowerPC 601, which has been in development for over a year, are being released by IBM. The PowerPC is a family of microprocessors created collectively by the three companies. The four new systems are designated the PowerStation 25T, PowerStation 25W, PowerServer 25S, and PowerStation/PowerServer 250. Each system runs the AIX/6000 Version 3.2.5 operating system, which is compatible with all existing RISC System/6000 systems. As a result, applications developed for the RS/6000 system will run on the PowerPC-based platforms without any modifications. All of the products employ the 601 processor, which operates at 66 MHz to achieve SPEC-integer and floating-point ratings of 62 and 72, respectively. For more information, contact your local IBM office. RN

MODEL LEARNER SPEEDS LIBRARY DEVELOPMENT

A recently developed model-generation technology will help silicon foundries speed ASIC library development. The Master Toolbox library-generation software, designed by GenRad Inc., Concord, Mass., works by learning existing cell models. The "model learner" automatically acquires cell data, such as functionality, propagation delay, and violation checks, from existing cell models used in reference analog or digital simulators. It then places this information in a neutral database. Using this information, the software generates the simulation model and verification stimulus for a variety of popular design environments. The resultant models are simulated and verified in their native environment to ensure accuracy. Up to 100 ASIC cells can be created in a day with this automated process. Master Toolbox generates models in several formats, including QuickSim II, System Hilo, Verilog, VHDL, and synthesis formats. For more information on the Master Toolbox modeling technology, call (508) 369-4400. LM

TECHNICAL PAPERS PROBE LOGIC-SYNTHESIS KINKS

A collection of papers to be presented at the International Conference on Computer-Aided Design (ICCAD) will explore some of the difficulties involved in using both combinatorial and sequential logic synthesis. For instance, a serious drawback for combinatorial synthesis lies in the use of ordered binary decision diagrams (OBDDs). With OBDDs, programmers must devise algorithms to order the variables. However, these heuristic ordering algorithms inhibit OBDD operations from being completed within a limited amount of memory. An ICCAD technical paper proposes software that determines and maintains variable ordering by dynamically applying a minimization algorithm that reorders the variables during OBDD operations. In another paper, a new model provides a canonical form for sequential functions. With the model, designers can approach sequential and parametric functions in a fashion analogous to using binary decision diagrams for combinatorial functions. Other topics at the conference include analog modeling, simulation, and synthesis; process and device modeling and simulation; placement and floorplanning; and system-design issues. ICCAD will take place November 7-11 at the Santa Clara Convention Center in California. For more information, call the conference's organizers, MP Associates, at (303) 530-4562. LM

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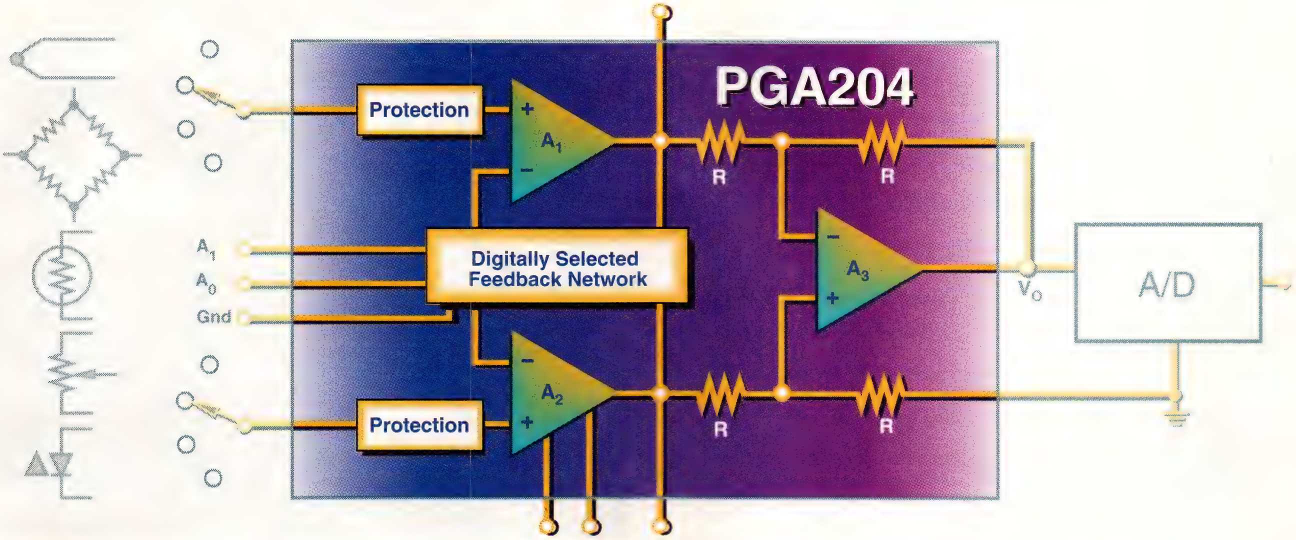

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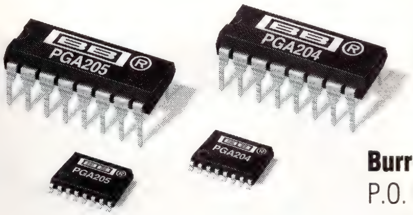

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PROGRESS REPORT

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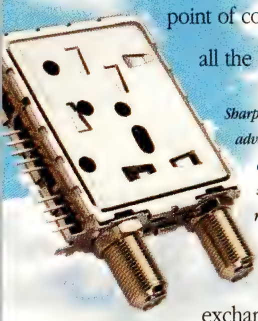
The TV set is the most likely point of confluence for all the innovations in information exchange now converging on the home market, with every media from video disks to fiber optic highways jostling for position. At Sharp, we've always been partial to the path of least resistance — the airwaves — ever since we created and marketed the first mass-produced crystal radio sets back in 1925.



Sharp's ultra-compact DBS tuners — with their advanced designs, reduced component count and low power consumption — contribute to smaller system sizes and have established new paradigms for reliability and integration.

You might be surprised at the number of areas in which Sharp continues to be the pacesetter in wireless communications components. Whether your transmission is in RF or IR bandwidths, by terrestrial or satellite broadcast, across the continent or across the room, here's why it pays to have Sharp go to bat for you.

H/V linear and R/L circular polarization LNBs from Sharp provide superior cross-polar discrimination, plus a waterproof, airtight structure which ensures reliable performance in the most severe conditions.

A FINE LINE OF RF COMPONENTS, FINE-TUNED TO YOUR NEEDS.

For years, Sharp has led the field in the miniaturization, noise reduction and seamless integration of RF components, from Ku band LNBs — the industry's smallest — to 22cc DBS tuners. The breadth of Sharp's line and our ability to custom-configure help us meet your size, packaging or power requirements readily.

As North American DBS comes into its own, we'll be there to bring home whole *new* generations of products supporting, for example, the transmission of multiple signals and vast home programming options — the products of *your* imagination.

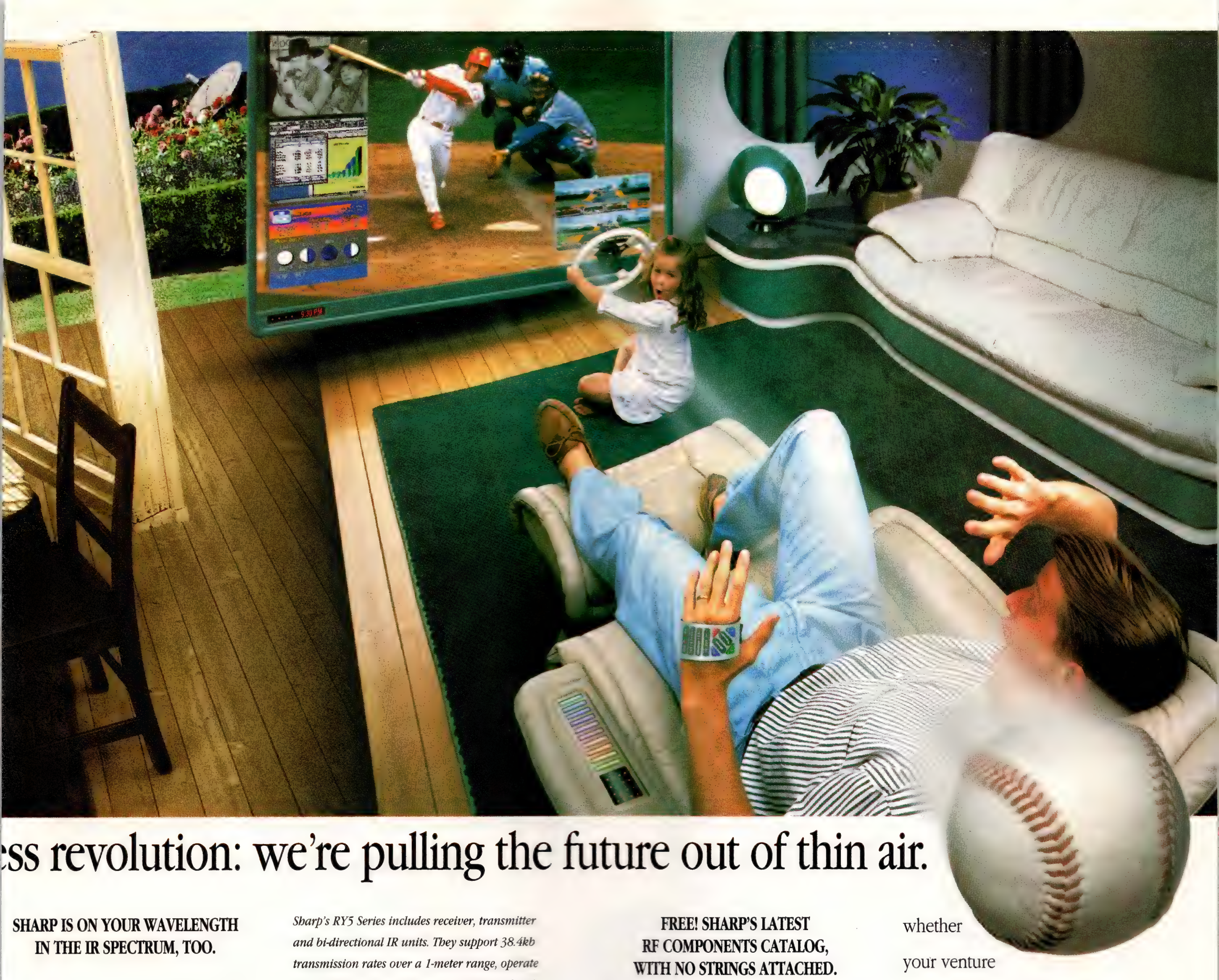
From the crystal radio to the wi

WE BRING TV SIGNALS TO THE HEART OF YOUR COMPUTER.

Sharp's flat-mount TV tuner/demodulator features a 55 - 801 MHz tune range and demodulated NTSC video and audio outputs. A pin-compatible PAL version of the module will also be available, based on a 5.5 MHz intercarrier frequency.

It should come as no big surprise to see that Sharp, the world's leading manufacturer of RF components, is one of the first to deliver a TV tuner/demodulator in a flat-mount package offering easy integration in system design.

It's the start of a whole new ballgame. Manufacturers of desktop and portable PCs gain immediate entry into video and multimedia — two arenas where tuner size, mounting and power requirements precluded their entry until now. And because this is a complete component modu they can avoid design and development at the subassembly level — always an enviable competitive edg



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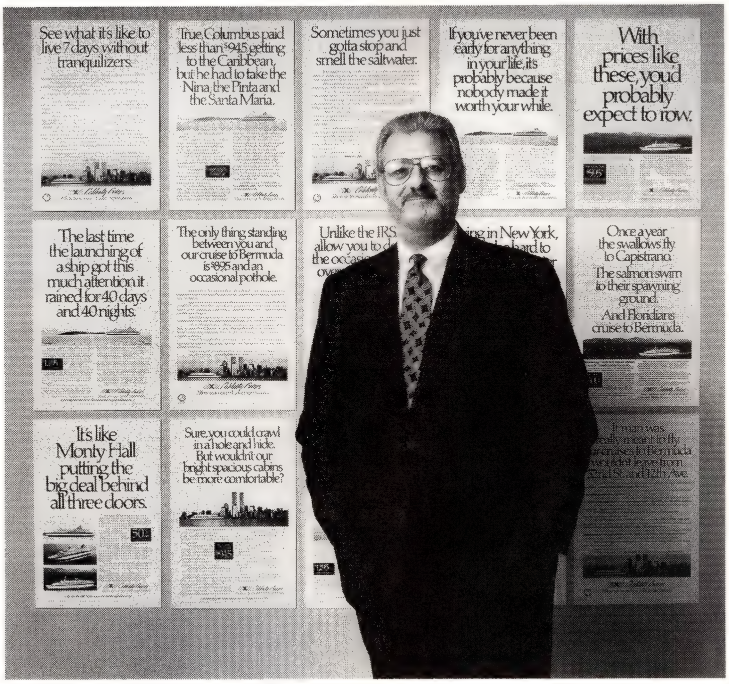
See what it's like to live 7 days without tranquilizers.
True, Columbus paid less than $945 getting to the Caribbean, but he had to take the Nina, the Pinta and the Santa Maria.
Sometimes you just gotta stop and smell the saltwater.
If you've never been early for anything in your life, it's probably because nobody made it worth your while.
With prices like these, you'd probably expect to row.
The last time the launching of a ship got this much attention it rained for 40 days and 40 nights.
The only thing standing between you and our cruise to Bermuda is $895 and an occasional pothole.
Once a year the swallows fly to Capistrano. The salmon swim to their spawning ground. And Floridians cruise to Bermuda.
It's like Monty Hall putting the big deal behind all three doors.
Sure, you could crawl in a hole and hide. But wouldn't our bright spacious cabins be more comfortable?

Photo: Frank Moscati

Al Wallack, Sr. VP Marketing, Celebrity Cruises, after returning from having his hearing checked.

"A great time to introduce a new luxury cruise line. The economy was in a slump, and the competition was on the rise.

We told our new advertising agency we have to go in with all guns blazing. And gave them the extra money to do it.

They recommended a three phase campaign. Phase 1. Full page newspaper. One ad a week for 24 weeks and one-third pages in the travel section. Phase 2, radio. Then 3, television to sweep up one season and sow the seeds for the next.

To make a long story short, two-thirds into the newspaper phase, Celebrity's ships were just about full to the end of the season. With so little left to sell, we all agreed to hold the radio and TV and save the remainder of the budget.

In roughly two years Celebrity became the number one cruise line from New York to Bermuda.

We've just added another new luxury ship and we're anxious to fill it. So once again we've upped our budget. So far, our agency hasn't tried to talk us out of it."

AAAA

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Automatic-test-equipment (ATE), wireless-receiver, data-compression, and telecommunications applications are perpetually in need of high-performance bipolar transistors. Complementary processes for analog tasks have been developed over the last few years to meet those needs. But resultant devices were relatively expensive because many of these processes were developed from the ground up at high cost.

Designers at Tektronix Corp., Beaverton, Ore., however, took a different approach by building a high-performance complementary analog bipolar process based on an existing wideband/high-speed analog process. This provides what the company claims are the most economical high-performance devices for the aforementioned applications.

The new complementary Pi or C-Pi process is an enhancement to the company's earlier npn-only junction-isolated (JI) bipolar Super Hi Pi or SHPi process. Whereas SHPi supplies 8.5-GHz npn transistors and lateral pnp transistors with modest f_ts, C-Pi offers vertical pnp transistors with an f_t of 5.7 GHz, and the npn transistors now operate at 9.2 GHz. Furthermore, a second-generation tile array also was developed to provide users with greater flexibility.

Like the earlier SHPi process, C-Pi consists of an analog technology and its inherent additional process complexity and associated cost. That's because among other characteristics, its transistors must have a higher breakdown voltage (BV_{CEO}) and a better beta Early-voltage (BV_A) product than a "digital" (say for ECL) transistor with the same f_t. Early voltage is a direct function of breakdown voltage. As is commonly known, if f_ts climb and feature sizes drop, BV_{CEO} also drops.

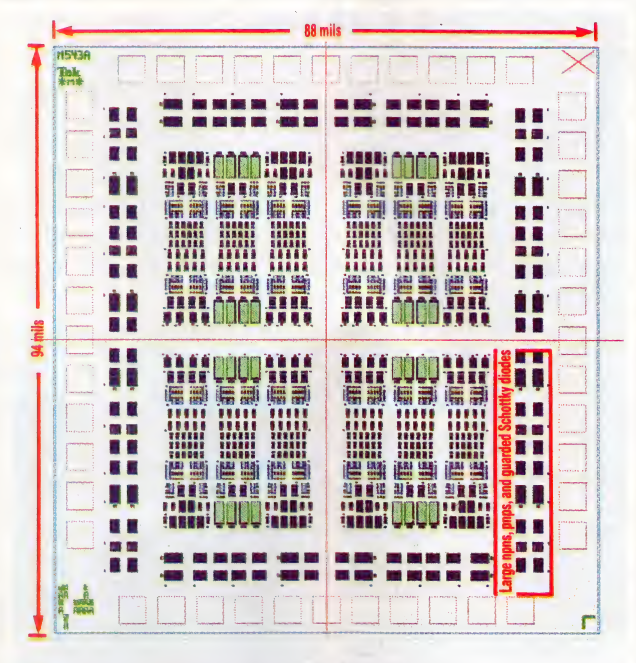


Figure 1

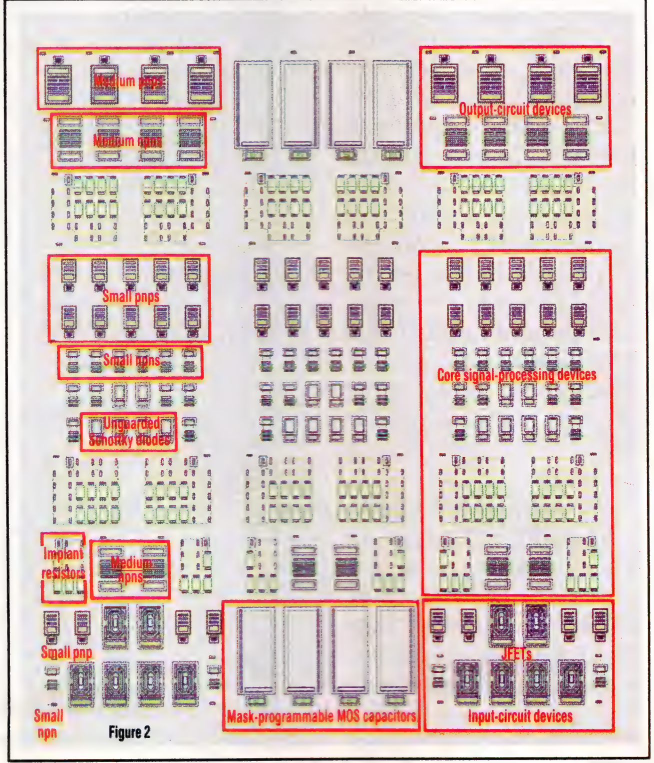


Figure 2

Many transistors that are comfortable running in high-speed ECL circuits couldn't operate in basic analog circuits. Ideally, a good analog transistor should have a BV_A product of 2^n, where n, expressed in bits, equals the accuracy of the circuits to be built. Thus, Tektronix's process designers were faced with getting the new pnp transistor BV_A as close as possible to that of the npn transistor without cutting BV_{CEO} below its present level of 12 V (a typical ECL transistor might have a BV_{CEO} of 8 V).

Not only did the designers come up with a higher f_t of 9.2 GHz for the npn transistor, but they also combined it with a BV_A product ranging from 750 to 3520 (device to device). Moreover, the new pnp transistor was brought in with its significant f_t of 5.7 GHz, combining it with a BV_A product ranging from 220 to 520.

Note that since B is dimensionless and Early voltage is basically a figure of merit, they along with BV_A are expressed without units. Breakdown voltages were kept at their proper levels, with the pnp transistor running slightly higher, as is the usual case. The BV_{CEO} of the pnp transistor runs between 9 and 13 V, while that of the npn transistors runs between 8 and 12 V.

In addition to the fast bipolar transistors, the process also provides JFETs with a G_m/C of 600 MHz, and metal-mask programmable MOS capacitors. It also supplies implanted resistors with a sheet resistance of 80 or 1350 Ω/square, as well as 50-Ω/square NiCr thin-film resistors (which offer laser trimming as an option).

To simplify the use of C-Pi for IC design, Tektronix's engineers created a simple but very carefully populated and laid-out complementary bipolar array *(Fig. 1)*. The second-generation tile array, measuring 88 by 94 mils, is made up of four identical macro tiles located symmetrically about the chip's horizontal centerline. The tiles' small-signal input circuits are located along this centerline, while the output devices at the top and bottom of the tiles are located close to the I/O.

The four tiles are surrounded by a dual ring of large pnp and npn transistors and "guarded" Schottky diodes. Placed between the small-signal circuits in the arrays and the 46 bonding pads, the large pnp and npn transistors are ideally located to perform their I/O functions. Analog circuits use "large" transistors on their inputs to minimize noise. And, all circuits benefit from the large output drive provided by such transistors. The Schottky diodes provide electrostatic-discharge protection. In all, 304 npn and 216 pnp transistors populate the chip.

The small, medium, and large pnp transistors are rated at collector currents of 0.95, 3.75, and 16 mA, respectively. The npn transistors are rated at 1.25, 5, and 20 mA, respectively. That's at maximum f_t and 4 V between collector and emitter.

Each tile is laid out in functional "microtiles" to simplify signal flow from input to output *(Fig. 2)*. The first two rows contain the chip's dozen JFETs, four MOS capacitors, and several small-signal npn/pnp transistors. The JFETs are located there so they can operate as input buffers. Above them lie implanted resistors and a few medium npn transistors, followed by more resistors and more small npn and pnp transistors. The top three rows contain devices to build the drive circuits for the output transistors, They include implant resistors, medium-size npn and pnp transistors, and four additional MOS capacitors.

For additional information, call Carole Hiscox at (503) 627-5560.

FRANK GOODENOUGH

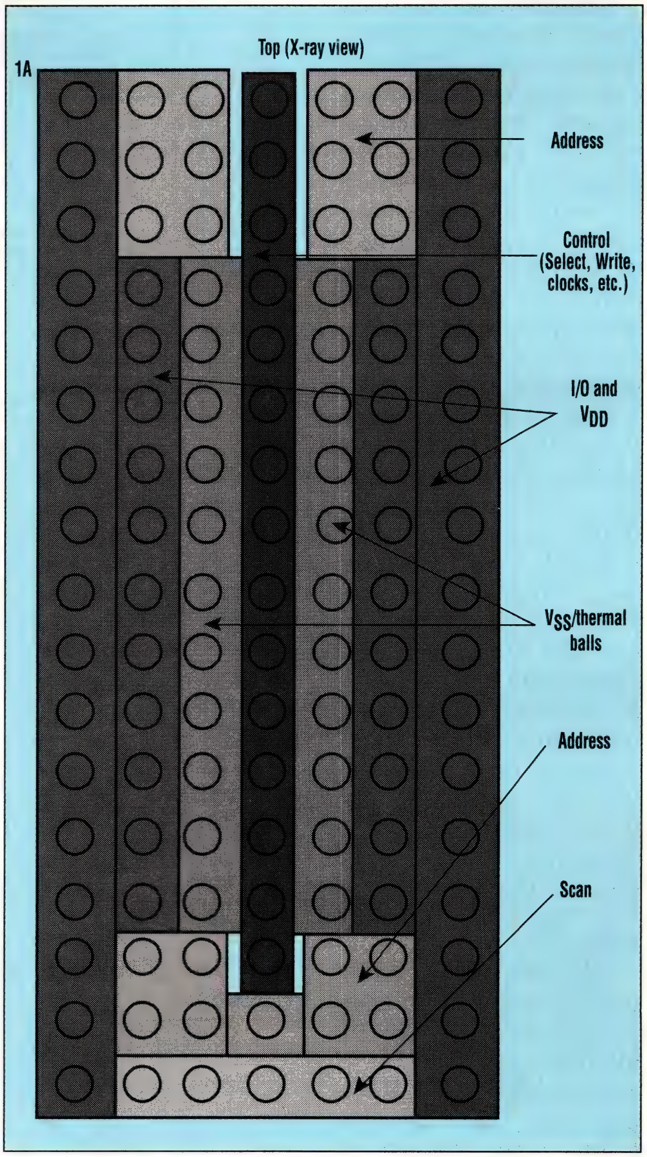
BGAs Make Transition To Memory Packages

The ball-grid-array (BGA) package, whose advantages have been touted for large-pin-count packages since its commercial arrival last year, is now beginning to move into relatively low-pin-count packages for fast static RAMs (FSRAMs). Motorola's Semiconductor Products Sector, Austin, Texas, has found that the same electrical, thermal, and mechanical features that make its BGA package, the overmolded pad-array carrier (OMPAC), useful as a gate-array package also lend themselves to packaging high-speed memories.

Motorola's foray into packaging FSRAMs in the OMPAC began with the development of a semicustom part for one of the company's radio-telephone products. According to David Chapman, product planning and applications manager for FSRAMs, the telephone's designers required a very thin memory package and decided that they liked the OMPAC. "The further we got into it (the project), the better the package looked," says Chapman.

With application-specific memory packages already growing in pin counts, the FSRAM group in Austin was already fishing around for an alternative to standard small-outline packages. That's where the OMPAC enters the picture, because it has room to expand into higher I/O counts as memories take on functionality and increase in word widths.

Enlarging the pin counts with standard memory packages like a thin small-outline package (TSOP) is reaching its practical limits in thermal terms. According to Chapman, the OMPAC neatly addresses thermal concerns. "There's no other package in this price range that approaches the thermal performance of BGAs," explains Chapman. "We expect to see, in the long run,



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better than 20°C/W performance on these sorts of packages." The key to the OMPAC's thermal performance is its incorporation of thermal vias. The vias run from the back of the die down to bumps on the package, which in turn are tied to the ground or power planes of the pc board.

The OMPAC's electrical capability lends itself well to packaging high-speed memories. The package houses a pc-board-like substrate that carries circuit traces on both sides, which enables packaging of substrates with transmission-line traces that run straight out to the solder pads. This facilitates the packaging of future memories running at speeds exceeding 200 MHz.

Although the bondout from the chip is a peripheral wire bond, Chapman foresees BGAs as a transitional technology into bumped die. Eventually, FSRAMs with bumped die will be packaged in OMPACs for even more speed and lower parasitics.

The FSRAM group has also found that the OMPAC lends itself to a standard pinout. Chapman is working on a scheme in which the package's unique I/Os, such as the Write Strobe, Chip Select, and clocks, would be laid out down the middle column. Duplicate functions would be laid out as mirror images across the spine *(see the figure)*. With such a pinout (or bumpout, in this case), layout for a double-sided board is easier. It obviates the need for identical memories with different part numbers for reverse lead pins.

The standard bump pattern being developed will be an array of 7 by 17 for 1-Mbit through 16-Mbit SRAMs in by-9 through by-36 configurations. To achieve a by-72 configuration, Motorola will go to a 9-by-17 bump array. Memories are expected to appear in this package style by late 1994.

As of now, Motorola is offering two memories in the OMPAC. One, the MCM67Q709, is a 128-kword-by-9-bit memory fabricated on the company's silicon-gate biCMOS technology. The other, the MCM56824AZP, is an 8-kword-by-24-bit device that's designed for direct connection to the company's DSP56001 digital-signal processor. Both come in an 86-bump OMPAC on a 9-by-10 grid.

Future OMPAC-housed memories may include a 64-kword-by-18-bit memory that's now available in a PLCC. In the longer term, the company expects to offer a series of 1-Mbyte, 4-Mbyte, and 16-Mbyte devices in configurations from by-9 through by-72. Their targeted speed is 150 MHz or more.

The JC-42.3 committee of JEDEC is currently considering possible BGA pinouts for SRAMs. Interested parties are encouraged to participate in the standard's development. For information, call Motorola's FSRAM marketing at (512) 928-4141.

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Speech-Recognition Algorithm Cuts Memory, Boosts Accuracy

Speech recognition is the core technology of speech-activated systems—machines that convert the spoken word to text and control systems that respond to oral commands. However, available speech-recognition software falls short in one critical performance area: It can't recognize speaker-independent, continuous speech with a high degree of accuracy. Moreover, large amounts of memory are needed for operation on various computer platforms.

An advanced speaker-independent, continuous-speech-recognition algorithm, designed by Lernout & Hauspie Speech Products, a developer of multilingual voice-I/O technology in Woburn, Mass., overcomes these problems. In a recent test conducted on a standard computer platform equipped with a digital-signal processor, the algorithm exhibited accuracy rates of up to 96.7%, while reducing memory requirements to about 7% of equivalent systems. The test was run on a database provided by the National Institute of Standards and Technology.

This performance is due to the combining of artificial neural networks (ANNs) with the company's phoneme-based Hidden Markov Model (HMM) technology. HMM technology models phonemes as opposed to words. Phonemes are the basic sounds in any given language. Typically, a language will contain only 40 to 50 phonemes. To recognize large vocabularies, or add or change vocabulary words without time-consuming retraining of the speech-recognition system, phoneme-based technology offers faster, more accurate performance with smaller storage requirements than first-generation, word-based systems.

Although phoneme-based technologies using HMM models are ideal for larger word and phrase structures, system accuracy is significantly lower when dealing with short phrases, including letters and digits. ANN technology adapted for speech-recognition systems combats this problem by providing a good trade-off between system complexity and accuracy for continuous speech as well as isolated words. Consequently, a speech recognizer combining HMM and ANN technologies performs a full range of speech-recognition functions with higher accuracy than systems based on just one of the two technologies. Unfortunately, such systems have been impractical due to the large amount of storage required.

Lernout & Hauspie's patented use of ANNs solves this problem by splitting an individual

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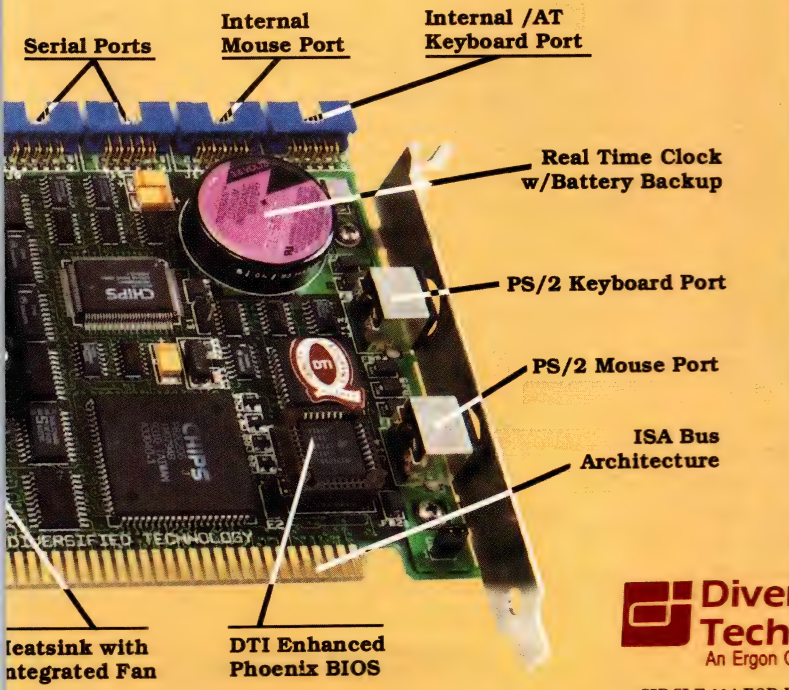
Serial Ports
Internal Mouse Port
Internal /AT Keyboard Port
Real Time Clock w/Battery Backup
PS/2 Keyboard Port
PS/2 Mouse Port
ISA Bus Architecture
leatsink with ntegrated Fan
DTI Enhanced Phoenix BIOS

FUNCTIONS	CAT3001 PENTIUM	CAT1070 80486	CAT1012 80486	CAT1011 80486
60MHz PENTIUM	✓			
50MHz 486DX		✓	✓	
50/66MHz 486DX/2		✓	✓	✓
33MHz 486DX/SX		✓	✓	✓
VGA True Color w/BitBlt		✓		
Up to 512Kb PROM/FLASH Disk		✓		
Up to 512Kb PROM Disk				✓
16Kb Integrated Pipeline Cache	✓			
128Kb/512Kb WriteBack 2nd Cache	✓			
64Kb/256Kb WriteBack 2nd Cache		✓	✓	
8Kb Internal Cache		✓	✓	✓
Up to 128Mb DRAM Onboard	✓			
Up to 64Mb DRAM Onboard		✓	✓	
Up to 32Mb DRAM Onboard				✓
2 Serial Ports / 1 Parallel Port	✓	✓	✓	✓
IDE/Floppy Interface	✓	✓	✓	✓
PS/2 Mouse Support	✓	✓	✓	✓
/AT-PS/2 Keyboard Support	✓	✓	✓	✓
Manufactured In-House(USA)	✓	✓	✓	✓
Powermeter 1.2 MIPS-60MHz	40.2			
Powermeter 1.2 MIPS-50MHz DX		22.4	22.0	
Powermeter 1.2 MIPS-50MHz DX2		21.7	19.9	19.6
Powermeter 1.2 MIPS-66MHz DX2		28.7	26.5	22.4

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ANN into several subnetworks, which then analyze the given speech structures. As a result, a smaller number of speech outputs have to be processed. This reduces the storage requirement while yielding the combined benefits of the two technologies.

The algorithm's patent was coauthored by Lernout & Hauspie and the International Computer Science Institute of Berkeley, Calif., and granted by the World Intellectual Property Organization. The software will be licensed. For more information, call Bart Verhaeghe at (617) 932-4118.

MILT LEONARD

INTERCONNECT SPECIFICATION BOOSTS PC MULTIMEDIA

Performance bottlenecks, the high cost of implementation, and installation difficulties—all have played a part in inhibiting the widespread adoption of multimedia on PC platforms. But these problems may now become moot with the Shared Frame Buffer Interconnect (SFBI) specification. The open interconnect specification will combine full-motion video, graphics, and other multimedia functions into a single subsystem for the PC platform.

Authored by ATI Technologies Inc., Thorn Hill, Ontario, Canada, and Intel Corp., Santa Clara, Calif., the SFBI allows memory to be shared between multiple controllers to form one low-cost graphics and video subsystem with enhanced performance. SFBI defines a memory organization and arbitration protocol that makes it possible for video and graphics to share one memory buffer. The specification also defines a common application-program interface (API), which allows developers to write applications using the shared-memory and ATI's SynchroLink capabilities.

SynchroLink is a technique that enables dedicated controllers in multimedia subsystems to communicate and synchronize time-critical I/O activities without host-processor intervention. These products, along with Intel's Indeo video technology, are expected to further push video as a standard feature for PCs.

By dismissing the need for separate video and graphics memory, SFBI-based implementations will reduce overall system cost. Additional savings result from eliminating extra circuit-board area, cabling, and other redundant hardware.

The SFBI-specified memory bus runs independently of the system bus. It can handle the task of manipulating raw uncompressed data at rates in excess of 20 Mbytes/s. With a sustained bandwidth of 140 Mbytes/s and a peak rate of 200 Mbytes/s, SFBI can handle full-motion video data while letting the system bus dispense with other functions.

The SFBI specification will be available from ATI and Intel free of charge. For more information, call ATI's Andrew Clarke at (416) 882-2600 ext. 8491, or Intel's John Thompson at (408) 765-1279.

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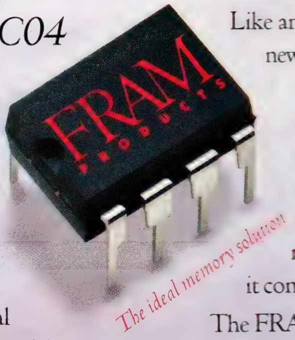

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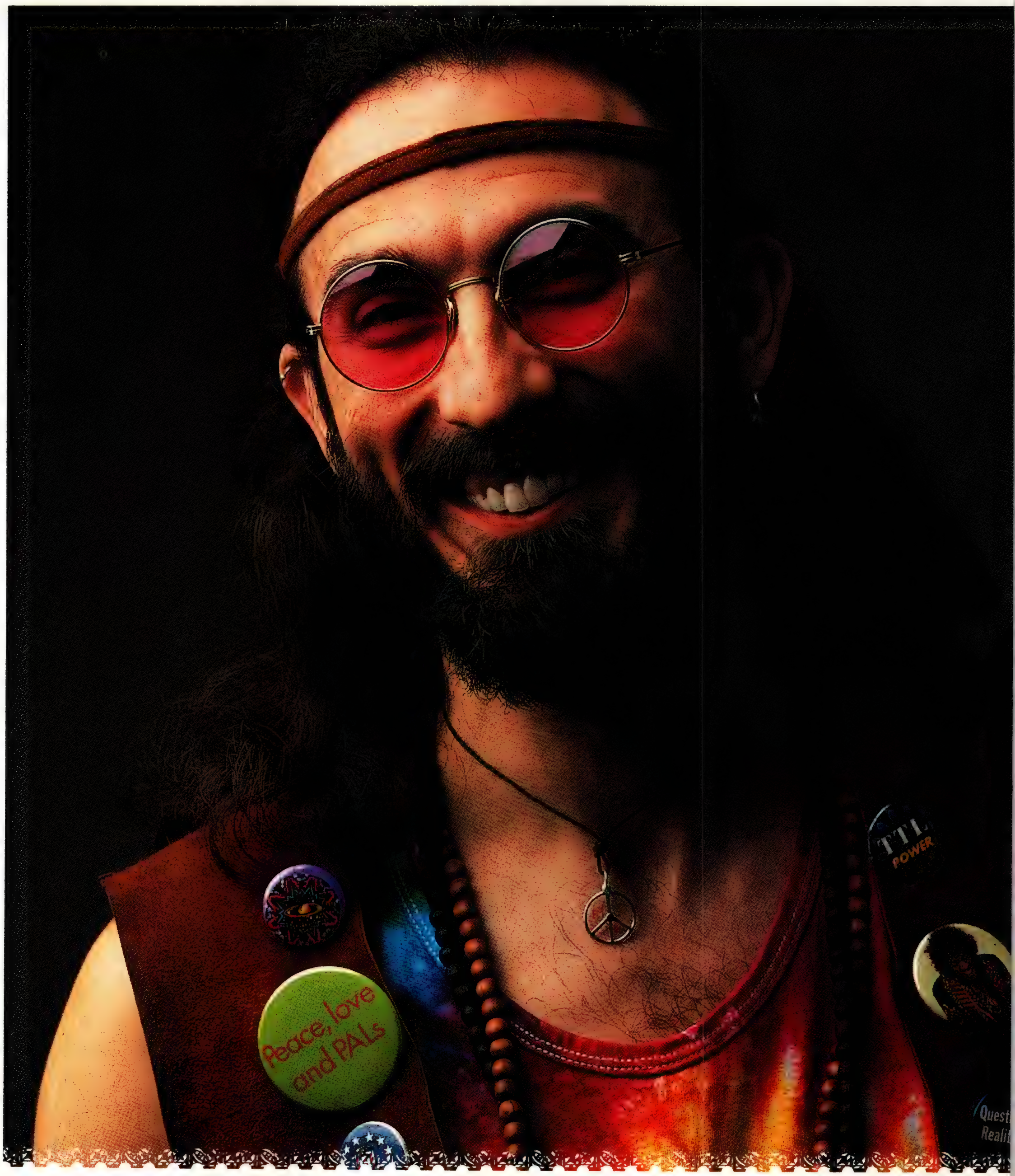

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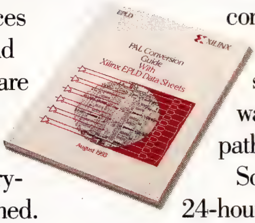

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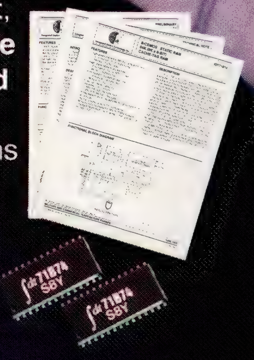

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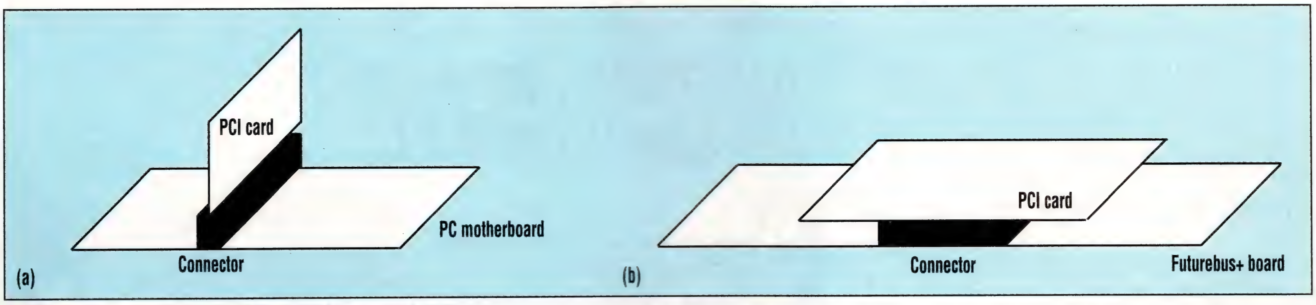


BECAUSE FUTUREBUS+ CARDS are placed in parallel in a rack, there's little space between boards. As a result, the PC implementation of PCI doesn't fit (a). When using Futurebus+, the PCI boards must be placed in parallel to the base boards (b).

I/O TASKS FIND THEIR WAY ONTO THE PCI BUS

AS BOARD MAKERS CONVENE FOR BUSCON, FUTUREBUS+ GAINS TWO MEZZANINE STANDARDS: PCI AND SBUS.

RICHARD NASS

The push toward using the PCI bus on high-end boards, including Futurebus+ and VMEbus boards, offers further evidence that the line between traditional PCs and workstations is dissolving. PCI, a local bus that can connect to high-speed peripherals such as video and disk drives, was originally designed for use on PCs. But makers of high-end boards are starting to see the merit of using PCI and Sbus on those boards. Such boards will be on display at the upcoming Buscon trade show, Oct. 19-20, in Marlboro, Mass. Sparc-based Futurebus+ boards also will be on tap.

Including the PCI bus and Sbus mezzanine slots on their boards allows Futurebus+ and VMEbus designers to take advantage of the wide array of available mezzanine modules. Sbus modules are already quite numerous and PCI boards are just emerging. But, the PCI implementations won't work in PC applications. In this case, the PCI boards are positioned perpendicular to the baseboard. Because Futurebus+ and VMEbus boards are typically placed in parallel in a rack, the space between the boards is minimal. As a result, the PCI modules will connect to the baseboards by lying in parallel *(see the figure)*. Using this configuration, Sbus- and PCI-based Futurebus+ and VMEbus boards will still fit into one slot. It's possible to use existing PCI products with Futurebus+, but the physical dimensions would require multiple slots.

The PCI bus and Sbus offer similar features and performance levels but employ different electrical and logical layers. One advantage of Sbus is that it ties into the Sparc environment, allowing it to use the large amount of Sparc hardware and software already available.

More than 20 different types of mezzanine cards for VMEbus exist (with many cards available for each type). Recently, a group of board manufacturers tried to standardize a mezzanine architecture for the VMEbus. But with so many boards being produced and each manufacturer wanting its own product to become the standard, no single standard mezzanine connector for the VMEbus has taken hold.

Futurebus+, on the other hand, is still in its infancy, leaving the door open for a standardized mezzanine adapter like the Sbus or PCI bus. Companies behind the standardizing effort include AT&T, Digital Equipment, Ericsson, Force Computers, Motorola, and Nippon Telephone Telegraph (NTT).

SAME PCI

The PCI specification that's likely to become a Futurebus+ standard incorporates the same electrical and logical layers as in the PCI Revision 2.0 standard. The signal pins are mapped one-for-one on the two connectors. The only notable deviation from the standard is that it will use a new style of connector and have a different card size (roughly 75 by 150 mm or about 3 by 6 in.). Also, a more stringent operating-temperature range may take effect.

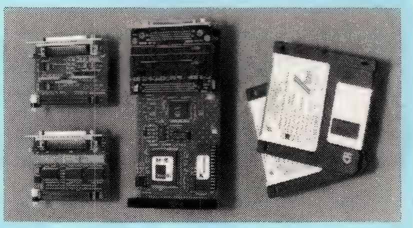
With the new PCI specification structure, a company that's already designed a PC-based PCI card can easily upgrade to a higher-performance baseboard. All that's needed to manufacture the same card for VME or Futurebus+ designs is to revamp the card's mechanical layout.

The entry by traditional personal-computer PCI-board suppliers into the VME or Futurebus+ market could in turn reduce prices because the PC community is typically accustomed to working with smaller profit margins. On the other hand, high-end board manufacturers can take advantage of the research and development that's already been done for the PC environment, using existing ICs.

The PCI standardization effort is broken into three groups, handled by three committees: the generic mez-

ADAPTER BOARD ACCEPTS FAST AND WIDE SCSI

Fast and wide SCSI is now available for Sun and Sun-compatible platforms using the PT-SBS440 SCSI-2 adapter. The adapter supplies a high-performance interface between the host and the 16-bit SCSI peripheral, typically a disk drive or drive array. The move to wide SCSI doubles the data throughput to 20 Mbytes/s. The adapter supports up to 15 devices. Single-ended and differential versions are available. The single-ended board uses the advanced forced-perfect-termination (FPT) scheme being written into the SCSI-3 specification. For simple installation, the adapter comes with Solaris 1.1 and 2.X software. The single-ended, 16-bit wide SCSI adapter sells for $995 and is available now.



Performance Computer Corp., *315 Science Pkwy., Rochester, NY 14620; (716) 256-0200.*

CIRCLE 496

REAL-TIME VME BOARDS EMPLOY RISC CPU

The RISCWorks Series of VMEbus systems is based on a derivative of the Mips R3500 RISC microprocessor. The three members of the family offer 3, 12, or 21 VME slots. Designed for real-time applications, the systems come bundled with the VxWorks real-time operating system designed by Wind River Systems. Either a Sun or Silicon Graphics workstation can serve as a development host.

The host CPU in each system is a 40-MHz HKMIPS/V3500, which offers a peak performance of 40 MIPS and 15 MFLOPS. The chip contains 64 kbytes each of direct-mapped SRAM instruction cache and direct-mapped SRAM data cache. The system comes with 8 Mbytes of DRAM, 1 Mbyte of EPROM, on-board Ethernet and SCSI ports with direct-memory access, two programmable timer-counters, a real-time clock, and four serial ports.

The 3-slot system is housed in a 4.75-in.-high enclosure, equipped with a 200-W power supply. The 21-slot model employs a 1000-W supply in a 17-in. case. And the 12-slot system comes with a 600-W power supply that's built into a unique 15-in. housing. The enclosure uses an inside-out modular architecture in which all key subsystems, including the drives, CPU boards, cooling assembly, and backplane, are mounted to an internal core chassis. As a result, the subsystems can easily be replaced or upgraded in the field. The RISCWorks/03, /12, and /21 real-time systems sell for $9959, $12,595, and $13,995 each, respectively.

Heurikon Corp., *8310 Excelsior Dr., Madison, WI 53717; (800) 356-9602 or (608) 831-0900.*

CIRCLE 492

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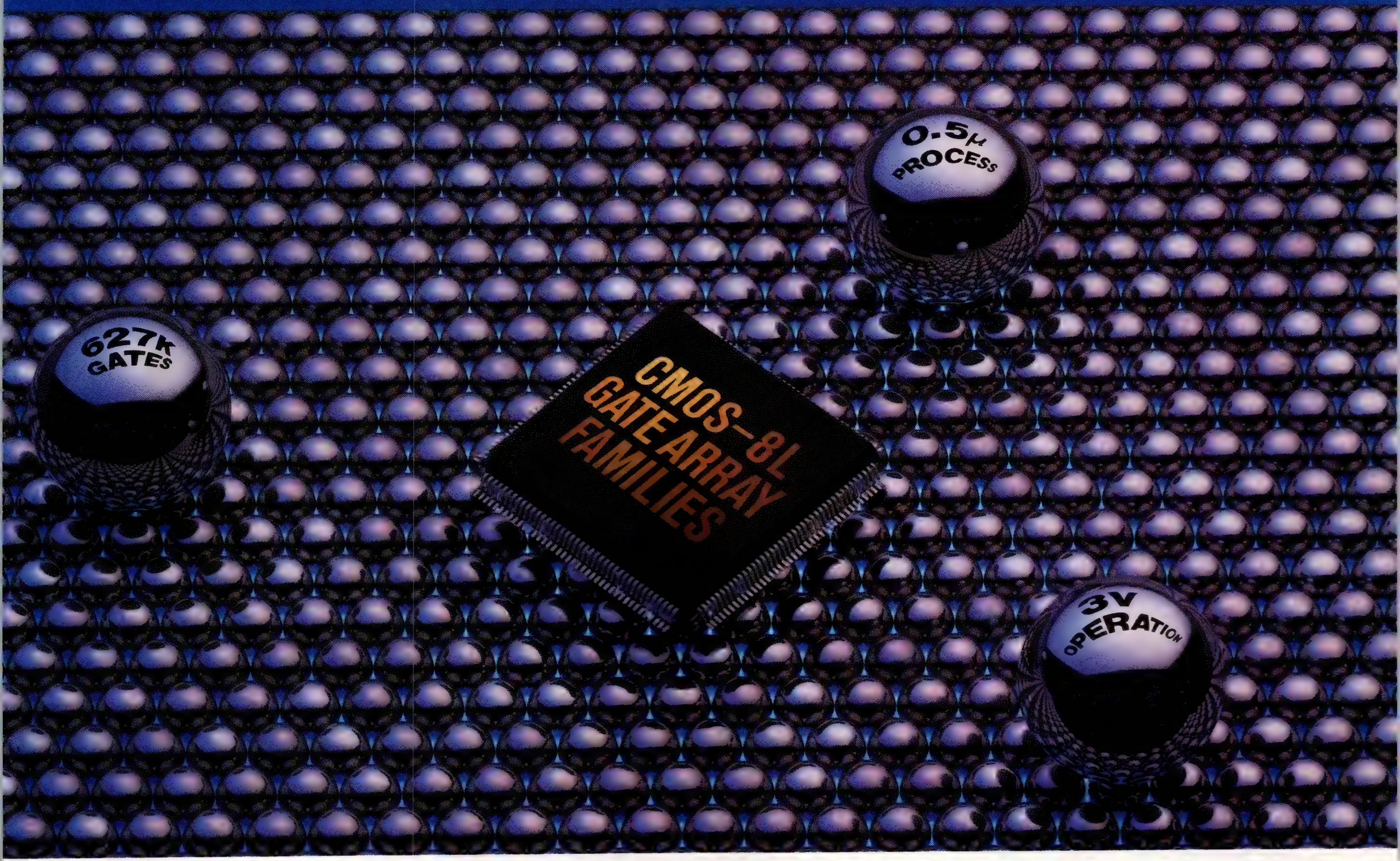

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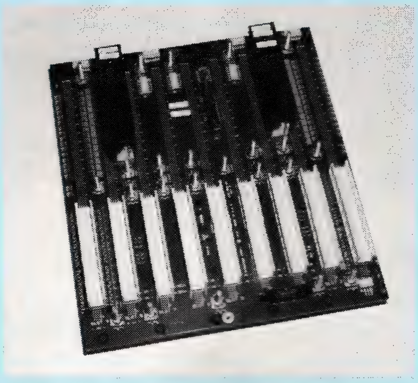
CIRCLE 251 FOR U.S. RESPONSE **CIRCLE 252 FOR RESPONSE OUTSIDE THE U.S.**

9-SLOT BACKPLANE HOLDS FUTUREBUS+ BOARDS

The 224 series of Futurebus+ backplanes has a new member—the 224-010 9-slot model. The series is built with a patented 2.1-V super-response termination power supply. This supply solves the 2.1-V noise problem cited by the Futurebus+ 2.1 Electrical Task Force.

Compliant with profiles A, B, and F of the IEEE 896 specifications, the backplane is available in 64- and 128-bit versions. The 14-layer design allows each connector row to be bused on its own signal layer in a fully shielded stripline design. Generous signal spacing, optimized trace width, and dielectric spacing contribute to high signal integrity, low propagation delays, and low crosstalk levels.



To get maximum signal transfers, the backplane is built using a 100% surface-mountable design and segmented power planes. Fully configurable geographic addresses and selectable delay encoders simplify system integration and debugging. The 64-bit version of the 224-010 Futurebus+ backplane is priced at $4150 each.

***Hybricon Corp.**, 12 Willow Rd., Ayer, MA 01432; (508) 772-5422.* **CIRCLE 493**

zanine-card (GMC) family that defines the overall mechanical structure; the PCI mezzanine cards (PMC); and the Sbus mezzanine-card (SMC) standard. The PCI specification will be the same for both VME and Futurebus+.

Digital Equipment Corp., one of the major manufacturers endorsing PCI, will employ the architecture as the local bus for its Alpha microprocessor. It's already employed in Intel Pentium-based designs and will probably be used with the PowerPC chip from Apple, IBM, and Motorola. Before year's end, DEC will announce a bus-independent PCI chip set that, although it's specifically designed for DEC's Alpha processor, will work with any bus.

ONLY PCI

DEC claims that PCI is the only mezzanine architecture the company will support on VME and Futurebus+. "It's so cost-effective and easy to work with that we think it's the right way to go," says John Giudice, DEC's program manager for boards. "We looked at all the different mezzanine architectures available and decided that PCI was the way to go. It didn't make sense to support Sbus because there's not going to be as many support chips available. There's already at least 30 companies working on PCI chip-set designs."

For limited I/O capabilities, the PCI mezzanine cards could reduce the number of Futurebus+ boards required for an application. But most designers working on Futurebus+ projects are looking to take advantage of the high-bandwidth I/O to move large amounts of data or graphic images. The Futurebus+ bandwidth and potential processing power (using multiple CPUs) offer much more than could be squeezed onto a PCI card. A 32-bit PCI adapter can typically sustain a 100-Mbyte/s bandwidth, while a 64-bit interface handles 200 Mbytes/s.

With the introduction of the Alpha processor, DEC will not only be selling systems to end users, but the company will make boards and chips available to OEMs. Alpha-based boards, using PCI, will debut for both VME and Futurebus+ in the spring of 1994, and volume quantities will ship by next June. The VME and Futurebus+ boards will come with different memory options. VME boards supported by VME64 carry 16 to 64 Mbytes of RAM in a single-slot 6U configuration. They'll start under $8000. Futurebus+ boards, in a single-slot 12U form factor (about 10 by 11 in.), will sell for under $15,000.

The company claims that in the next three to five years, almost every Alpha-based platform will use PCI as its native I/O bus. That would satisfy most applications, but special-purpose applications (such as multimedia) would require some sort of custom solution.

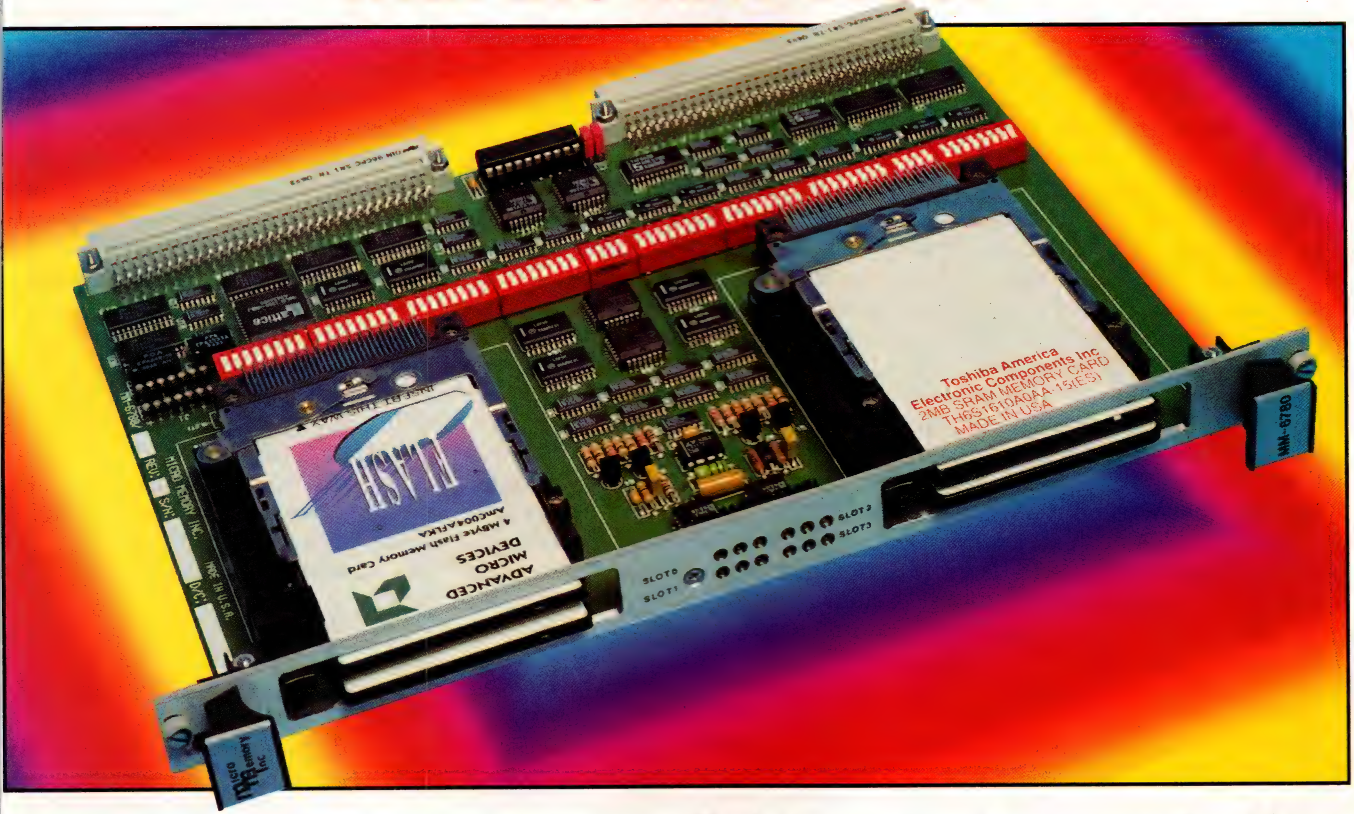
Futurebus+ itself has taken the long road to standardization. Michael Humphrey, Futurebus+ director of VITA, Scottsdale, Ariz. acknowledges, "At long last, some of these draft documents are finally reaching the end of their life. They're turning up in print, giving relief to

REAL-TIME OS GAINS UPGRADES

Version 4.2 of the PDOS real-time operating system contains enhanced task communications and management for such applications as high-frequency data acquisition, process control, and telecommunications. The task-communications functionality is achieved using multibit events, message-queue functions, counting and priority inheritance semaphores, and asynchronous system traps (ASTs). PDOS 4.2 is available in a development kit, which offers a suite of cross-development tools for PCs and Sun and HP hosts. License fees for the kit start at $3000.

***Eyring Corp.**, 1455 West 820 North, Provo, UT 84601; (801) 375-2434.* **CIRCLE 495**

UPGRADE VME SYSTEMS in a *FLASH* with the *MM-6780P*



PCMCIA flexibility allows insertion of up to four Flash or CMOS NVRAM memory cards in the MM-6780P VME Memory Module Adapter, with the power on. Upgrade your system by programming a new Flash Memory Card, unplugging the old one and installing the new one without turning off the power. Programs can be executed from the Flash memory or CMOS NVRAM with greater flexibility than an EPROM.

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CMOS NVRAM

MM-6740C	2M to 16M bytes, VME Error Detection and Correction
MM-6702C	512K to 8M bytes, On-Board Batteries

FLASH/CMOS NVRAM

MM-6790C	4M to 16M bytes, CMOS NVRAM; 4M to 8M bytes, Flash Memory VME/VME64
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people within the community. Futurebus+ is no longer a moving target. Now that the specification is settled, silicon is starting to appear and boards are starting to reach production."

A recent interoperability demonstration, which will be showcased around the country (although not at Buscon), brought together a number of Futurebus+ makers, including CCT, DEC, Force, Hybricon, Mupac, Nanotek, Schroff, Technabox, and Vmetro. Basically, the demonstration shows that board A can communicate with the memory on boards B, C, and D, thus giving the final proof that the technology works.

Futurebus+'s evaluation process will continue through this year and into 1994 as silicon becomes more acceptable. Packet-mode data transfers, which should soon be featured on Futurebus+, will offer a further performance improvement. This will give the bus even more exposure, especially in the military arena. Futurebus+'s telecommunications profile (Profile T) is nearly complete. It will be released before the end of this year and should be voted on in the first part of 1994.

QuickRing is another standardization issue brewing within VITA that will gain more momentum at Buscon. QuickRing operates with the VMEbus as a high-speed data mover for multimedia-type applications (ELECTRONIC DESIGN, *Oct. 1, p. 127)*. VITA is now a fully-accredited standards body recognized by ANSI, whose goal is to develop standards around VMEbus and Futurebus+.

Among the other issues to emerge from VITA in the near future are live insertion, fault tolerance, and asynchronous-transfer-mode (ATM) technology. DEC is involved in ATM projects using the protocols for communications, multimedia, and high-bandwidth messaging. IBM recently announced an ATM switch using the Autobahn spanceivers (serial-to-parallel transceivers). Autobahn is an architecture that allows data to be passed at 400 Mbytes/s using the serial lines on the VME P2 connector. Once Autobahn is running on copper media, it will move to an optical technology.

Eventually, optical technology may take over as the data-transfer method of the future, for several reasons. First, transmission-line effects become nonexistent as the reflections disappear. But the best reason is that optics has no glitches, simply because light doesn't act as a load. And the transmission speed increases by magnitudes because all problems associated with unbalanced lines and loads are eliminated. For example, light needn't be terminated. Instead, the cabinet's inside walls should be painted black so the light doesn't continue. A practical data rate employing optics is about 1 to 3 Gbits/s per channel using 16 receive and transmit channels. However, one problem with such a high-speed technology is that none of today's laser diodes can't switch that fast.

MULTIBUS II

Not to be overlooked, despite all of the PCI bus and Futurebus+ activity, are developments in Multibus II board technology. Over the last year, the key advances have zeroed in on software. Specifically, a driver was developed for the Windows DLL Transport, allowing standard, off-the-shelf, Windows software to be loaded and run. The driver and source code are available from the Multibus Manufacturers Group (MMG) for $495. With the software, a standard software environment can be integrated into a multiprocessing environment using Multibus II. This technology will be demonstrated at Buscon.

Other software that's in its early stages accommodates live insertion. The hardware capability was demonstrated a few years ago, but no one has yet developed a real product using the technology. Multibus II was the first bus out of the chute to implement live insertion. Futurebus+ is trying to execute the technique, and so far a few proposals have been put on the table. The next step for Multibus II is integrating the hardware and software into an application.□

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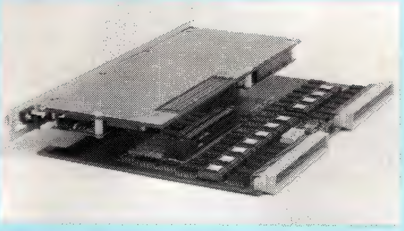
DSP AND DATA-ACQUISITION BOARDS MAXIMIZE FLEXIBILITY

A full complement of modular DSP and data-acquisition boards combine flexible analog and digital I/O options for real-time applications. The boards come with VME and VSB interfaces that accept up to three stackable daughterboards. As a result, the boards are suitable for such high-speed applications as radar and sonar, speech processing, communications, data compression, and embedded control.

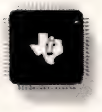
The Model 4200 features three different bus interfaces—VMEbus, VSBbus, and MIXbus. The 4201 eliminates the VSB interface, while the 4202 has just the VME interface. The 4200 and 4201 employ a Motorola 68030 microprocessor as the interface and multichannel DMA controller. Source and destination addresses, transfer type, and block-length parameters are accepted for each DMA channel. Available MIX modules include floating-point DSP cards, digital I/O, telecommunications interfaces, SCSI, and prototyping boards. Available now, the models 4200, 4201, and 4202 are priced at $2495, $1995, and $995, respectively. Large-quantity discounts are available.



***Pentek Inc.**, 55 Walnut St., Norwood, NJ 07648; (201) 767-7100.* **CIRCLE 494**

Which converter delivers twice the speed at half the power consumption in half the height?

TI's TLC320AC01 analog interface circuit.



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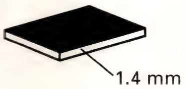
The 'AC01 is a fully programmable device that integrates 14-bit A/D and D/A converters, filters and I/O for a complete analog interface system.

The device combines twice the conversion speed with half the power consumption in half the height of TI's previous generation of AICs. This new generation is enabled by TI's advanced mixed-signal design methodology and 1-micron processing technology.

The 'AC01 interfaces directly with TI's leadership TMS320 digital signal processors (DSPs) and with other industry-standard DSPs and most general-purpose microprocessors.

TLC320AC01 At A Glance

- Low power consumption (100 mW) for portable systems
- Direct serial interface to most DSPs
- Shrink quad flat packaging (SQFP) available for low-profile, portable applications



- Single 5-V power supply for simplified system design
- 14-bit A/D and D/A converters and programmable filters
- Signal-to-distortion ratio: 72 dB
- TLC320AC01CFN 28-pin PLCC; TLC320AC01CPM 64-pin SQFP

And it can operate in three modes — stand-alone, master-slave and linear codec — for greater system-level design flexibility.

The 'AC01 can enhance the performance of your V.32 bis modem and PCMCIA card, speech and audio processing including multimedia, noise cancellation, industrial control and instrumentation designs.

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MCMs DEMAND A DFT STRATEGY

IN THE EFFORT TO MEET SUCH DEMANDS, DESIGNERS HAVE FOUND A NUMBER OF WAYS TO MAKE THEIR MULTICHIP MODULES EASIER TO TEST.

JOHN NOVELLINO

Design for testability (DFT) certainly isn't a new concept. Neither is the drive for concurrent engineering. But they are essential, particularly when it comes to the design and manufacture of multichip modules (MCMs). In the MCM arena, DFT and concurrent engineering—getting the design, test, and manufacturing disciplines working together from the start of a project—are mandatory to ensure an economically viable product and satisfactory yields.

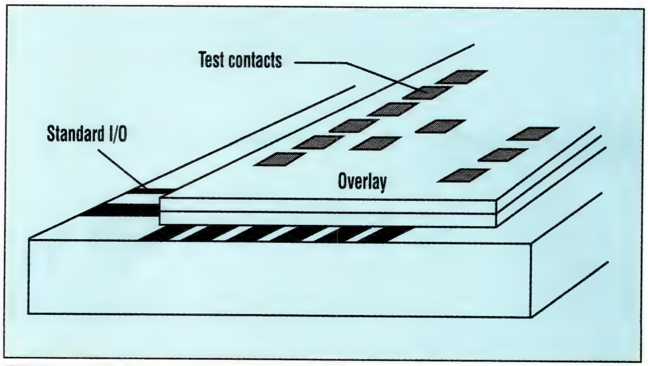
MCMs offer important size and performance advantages. But the small geometries that supply these advantages also create a test problem because access to test nodes ranges from very limited to nonexistent. The key components on printed-circuit boards (packaged ICs) can be thoroughly tested before mounting so that most failures will be caused by interconnect problems. On MCMs, however, the key components consist of bare die, which are difficult and expensive to test.

That raises the issue of known-good die (KGD), the buzzwords heard in nearly every conversation about MCMs. How can foundries and their customers assure themselves that they're shipping and receiving known-good die? Whose responsibility is it? Fortunately, techniques exist to create testable MCMs. But designers must take the time to evaluate a number of possible solutions before settling on one or more that suit the economics of their specific projects.

The importance of these questions is reflected in the technical program of this year's International Test Conference (ITC), which is scheduled for the Baltimore Convention Center from October 17 to 21 *(see "ITC '93: Putting it all together," p. 56)*. The ITC will present a session on "Multichip Module Testing," a tutorial on "MCM Testing Strategies," and a panel session called "Known Good Die: A Key to Cost-Effective MCMs."

REPAIRABILITY AN ISSUE

The decision on what type of testability techniques to use in MCMs is complicated by the fact that bad modules can be repaired. If a packaged chip is defective, it gets tossed. But if an MCM checks out bad before the cover is



1. MCMs fabricated using the High-Density Interconnect overlay process have a top surface that can be used for I/O pads and test pads. This can make internal nodes accessible.

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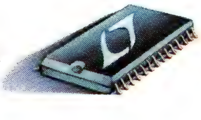
Buy A  Piece Of Our Technology And We’ll Give

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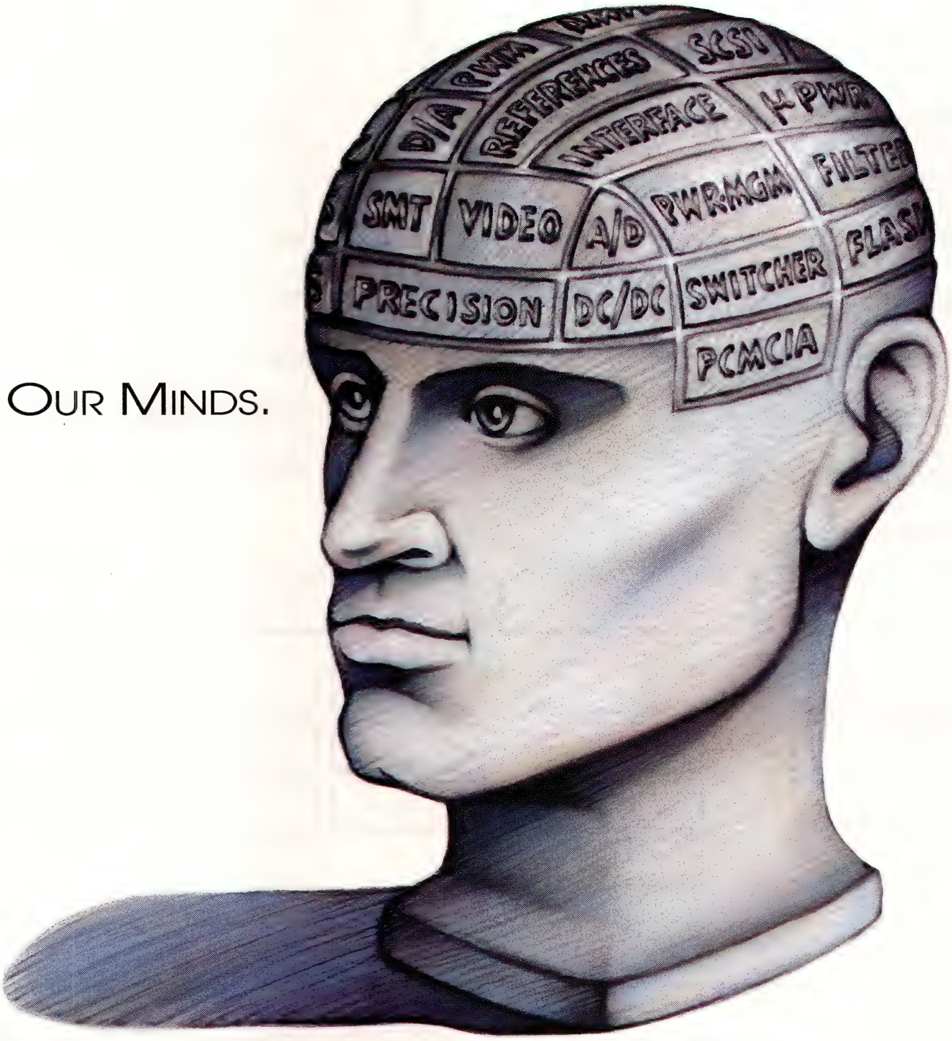

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- ANALOG SWITCHES
  - Low Power
  - Low Charge Injection
- LINEAR REGULATORS
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    - Fixed
    - Adjustable
    - Micropower
  - Negative Low Dropout
    - Adjustable
  - High Current
    - 3V Dropout
  - Logic Controlled
  - Power Surface Mount
    - SO-8, DD, SOT223, SOL-20
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CIRCLE 136 FOR U.S. RESPONSE　　**CIRCLE 137 FOR RESPONSE OUTSIDE THE U.S.**

BITE TEST PLAN

Test	Question
Continuity	Is the MCM making contact to the test socket?
Bus	Is each die installed in the correct location?
BITE/core	Are the die good? (Isolate the die I/O pads from the MCM's interconnect.)
Broadcast/Pattern	Are all die inputs and outputs properly connected to the substrate?
Standard die/non-BITE	Are the standard (non-BITE) die connected and working properly?
V_{oh} and V_{ol}	Are V_{oh} and V_{ol} drives correct?

put on, it may be economically possible to repair the device. That decision will depend on the cost of the module compared to the cost of a repair. Inexpensive modules will still be discarded, but that's becoming less and less the case, according to John Ferguson, product manager for multichip-module testing at Hewlett-Packard's Manufacturing Test Div., Loveland, Colo.

"If you look at the people who are making MCMs today and the marketplaces that they're breaking into, they're being used in military and aerospace applications. Those are very expensive parts, in general," says Ferguson. "The next big area that's opening up is in PC and workstation products. And once again we're talking about fairly expensive modules." Such modules may have a processor worth several hundred dollars, some memory, a memory-control chip, and other assorted devices, he notes. Total parts cost may be $1000, with any one device worth from $50 to $800, depending on the technology involved.

In this case, the design engineer must consider testability measures that offer diagnostic capability, which would reduce the cost of finding and replacing a bad die. "If the people doing the manufacturing and repair have no help at all, then the cost of repair will be higher than if the design engineer gives this some forethought and puts some things in place that might reduce that cost."

But the idea that repairability is of prime importance isn't unanimous. Although older MCMs had dozens of chips, the trend toward higher integration is making such high die counts unnecessary, according to Tushar Gheewala, president of CrossCheck Technology, San Jose, Calif. He points out that when you can get half a million gates on one chip, which is now possible, you don't need as many die on an MCM. In fact, he sees a trend toward modules with only two or three chips.

In the case of the larger modules carrying 50 or more die, the chances of assembling a good module the first time were small, says Gheewala. Hence, the need to be able to isolate the defective die and replace it was important. With smaller modules the rule in the future, he says, the chances of assembling a good module are pretty high—if the die are thoroughly tested first.

"So from the test perspective, in my mind the number one challenge for multichip modules is actually making sure that your bare die is tested thoroughly," says Gheewala. He goes on to say that in order to ensure KGD, wafer testing should look for opens and shorts as well as stuck-at faults.

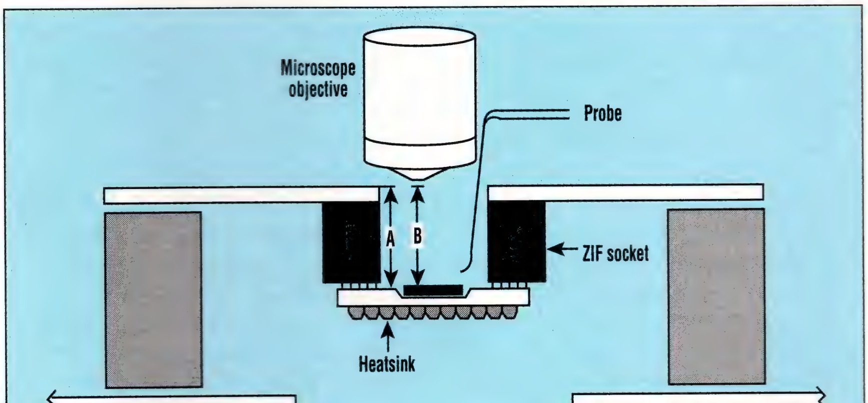
One technique that can help is I_{DDQ} testing. This method, which is gaining in popularity, exploits the fact that certain faults will cause quiescent current to change in a predictable way. The test can be run at the wafer level, and many ASIC vendors are beginning to support it, says Gheewala. The design requirements for I_{DDQ} testing aren't very restrictive. They basically involve making sure that the chip is free from structures that leak current statically.

Gheewala also boosts his company's proprietary technique, which embeds a test structure in the die's base array. The structure is a grid that offers a large number of observation points, and as such is conceptually similar to a bed of nails. Test patterns are automatically generated by CrossCheck's proprietary software. To designers, the device appears the same as a conventional ASIC. Performance doesn't change, and they use the same design process and CAE tools. A number of vendors now support the technique.

BOUNDARY SCAN A MUST

Once the KGD problem is solved to the designer's satisfaction, the most dominant fault type in an MCM will be structural faults—that is, bad interconnects. That's where boundary-scan testing comes in. Boundary-scan testing (IEEE-1149.1) is the interconnect test specialist. As useful as the technique is for testing crowded circuit boards, the demands of MCMs make it almost mandatory.

"Clearly, if there's something crying out for boundary-scan testing,



2. A PROBING TECHNIQUE for cavity-down devices employs a ZIF socket mounted upside down. A hole was cut in the socket for viewing the device and to insert a probe tip.

it's MCMs," says Peter Hansen, engineering manager at Teradyne's Assembly Test Group, Boston, Mass. "I think any designer making a digital IC that's going into an MCM should almost consider it a basic requirement to have 1149.1 support. I can't think of any reason why they would not want to do that."

Hansen notes that there are many chips available as bare die with boundary-scan circuitry built in. Most microprocessors now have the needed circuitry, and a number of bus parts are available. Designers can easily add boundary-scan support to any ASIC going into an MCM. The circuit still may end up with some non-scannable parts, but they can be included within the clusters that are tested as a group.

The design and execution of boundary-scan testing in an MCM is very similar to the board-level use of 1149.1. Typically, the testing would occur after the die have been mounted on the substrate but before packaging, says HP's Ferguson. Access would be through the pads, which will ultimately be connected to the package pins. These pads are large enough—usually on the order of 6 mils but even as large as 15 mils—so that it's possible to design fixtures to interface with them, according to Ferguson.

The boundary-scan test-access port can also be used to run various forms of built-in self-test (BIST) capability, which test the die before they're mounted in the MCM. A technique called built-in test equipment (BITE) is recommended by Robert Bone, manager of product development, engineering, and MCM operations at Hughes Microelectronics, Newport Beach, Calif. "Since the die is the heart of the logic system, the first focus of yield, testability, and diagnostic evaluation must start at the die level," says Bone. "The die must be tested in the same manner at each level of assembly. Otherwise, defective die can pass at the lower levels."

Although the basic concept is similar to BIST, the term BITE goes back to the 1960s when it was used in discrete devices. BITE is more hardware-oriented and gives the user a direct go/no-go answer from the chip, notes Bone. In contrast, BIST outputs a bit pattern that must be evaluated by an external tester. Fully implemented, BITE offers a thorough evaluation of the die *(see the table)*.

The BITE circuitry takes up about 10 to 15% of the die area, but Bone says that's quite cost effective, considering the test structures can be used throughout the system's life cycle. "Some people look at using even 1% of the chip area for testability as horrible," he says. "But they're primarily concerned with making chips, not making systems."

Hughes has successfully used BITE since 1989. Various forms of the circuitry have been employed in MCMs containing custom gate arrays, microprocessors, RAMs, EEPROMs, and other circuits. Typically, the modules measure 2 by 4 in., have 368 to 442 I/O pins, and contain three to six custom gate arrays and 20 to 24 standard non-BITE die.

Design verification is also an important consideration in MCMs. That prompted the development of a flexible prototyping method which uses an overlay interconnection approach to probe for verification. The High-Density Interconnect overlay process, as it's called, was described in a paper presented at last year's IEEE MCM Conference by Lynn E. Roszel of Texas Instruments, Dallas, Texas, and Wolfgang Daum of General Electric Corp., Schenectady, N.Y. Texas Instruments worked with General Electric and the Defense

ITC '93: PUTTING IT ALL TOGETHER

The myriad parts of the puzzle that go into a successful system design will try to be conjoined during the 1993 International Test Conference in the Baltimore Convention Center, October 17 to 21. The centerpiece is testing, of course, but 112 papers, 16 tutorials, and 8 panel sessions will thoroughly cover the relationship of testing to design, manufacturing, diagnostics, and standards.

Paper sessions emphasize such popular topics as I_{DDQ} testing, boundary-scan applications, IEEE-1149.X standards actions, design-for-testability (DFT) approaches for multichip modules, and structured system testing. Mainstream test and diagnostics issues include built-in self-testing, delay faults, synthesis, test-equipment hardware, and automatic test-pattern generation.

Controlling costs is critical these days, so the program includes a tutorial entitled, "Economic Issues in Test: Design Through to Field Test" and a panel session called, "DFT—Profit or Loss." The tutorial (number 16) will present the economic benefits to be gained by effective test programs and DFT techniques. The goal is to arm designers with information needed to convince management to support test strategies. In the panel session (number 12), industry experts will share their views on the cost-benefits equation of DFT from the standpoint of design, manufacturing, and field testing.

This year's keynote speaker, Joseph B. Costello, president of Cadence Design Systems Inc., San Jose, Calif., will discuss "Design & Test: What Will It Take to Tie the Knot?" Costello argues that electronic-design-automation suppliers have done such a good job facilitating the design of highly complex products that designers are producing untestable designs. He notes that EDA vendors must provide mechanisms to incorporate testing into the design process and create tight links to the test industry.

A special tutorial offered free to all registered attendees will discuss ISO 9000. Along with an overview of the standards, the tutorial will examine the benefits of ISO 9000 registration, the costs involved, and how the standards fit into the Total Quality Management philosophy.

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Advanced Research Projects Agency in Alexandria, Va. to bring the new process to industry as a merchant foundry.

The process differs from most other MCM technologies in that it builds the interconnect over the top of the bare die rather than placing the die on an interconnect structure. Vias are drilled through the dielectric to the die bond pads and then to the substrate I/O pads. To reduce prototype turnaround times, the process uses information from the CAD database to create the via-drill and interconnect patterns. The resulting overlay structure has a top surface that's available for I/O pads and test pads, which can be used to make internal nodes accessible *(Fig. 1)*. This added probing capability makes it easier for designers to evaluate the prototype's functionality and the interconnect structure's performance.

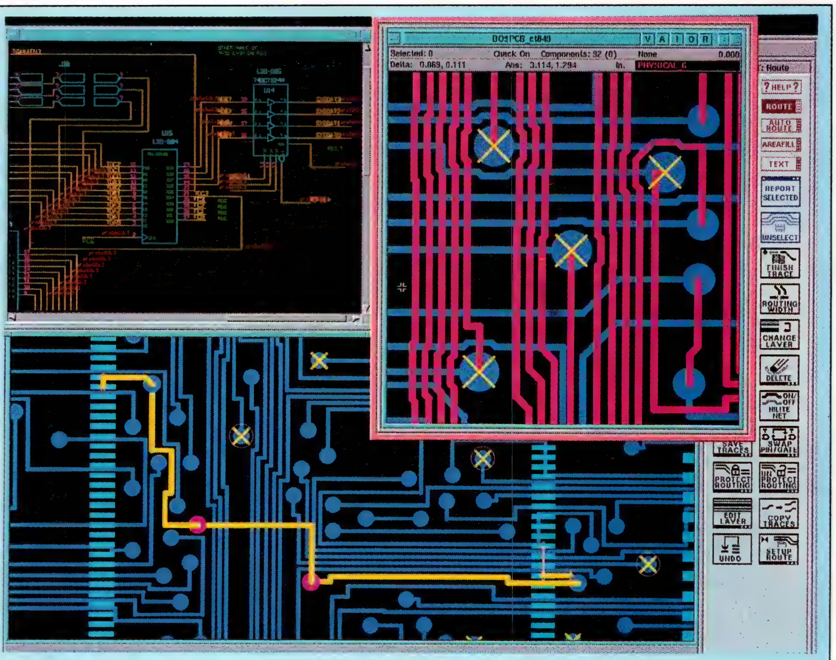
The earlier in the MCM design process that the design team begins working with the foundry, the more flexibility the overlay process can deliver. Roszel and Daum note that some system-level and detailed design considerations may be influenced by the ability to use the top-level pads for control and observation. In addition, the increased I/O capability of the top-level pads may allow an additional die to be included in the MCM package, eliminating an additional package or test-socket lead time.

Getting the foundry involved at or before part selection makes it possible for designers to use existing die. Using off-the-shelf parts means the die will have existing yield data, test vectors, and known performance.

In some cases, probing of certain critical nodes on the MCM may still be the best way to test the device, particularly during verification, but also for fault isolation. This may be the only way to check the adequacy of timing and voltage margins. In fact, probing the nodes would be the only way to do any type of analog evaluation of the signal. Fortunately, there typically are few critical nodes, and a single channel, perhaps connected to an oscilloscope, will usually suffice.

"I would certainly think that a designer would feel much more comfortable about releasing a design if he had a way to look at certain internal critical nodes," says Zoran Sekulic, marketing manager for MCM products at Integrated Measurement Systems (IMS), Beaverton, Ore. "If those nodes are hidden, he's taking a substantial risk. If they're accessible, then the designer can use some kind of manual probe to see if his timing margins and signal integrity are okay."

IMS used a probe technique to characterize a custom-formatter array IC that provides per-pin timing in the company's ATS digital tester.



DFT TOOLS AUTOMATE SCAN TEST-POINT SELECTION

Two design-for-testability tools help designers of multichip modules and printed-circuit boards containing boundary-scan devices create high-quality tests while reducing test-program development time and test-fixture cost.

"Virtual Test Manager: TOP" is designed around Teradyne's Victory boundary-scan technology and Mentor Graphics' Design Architect. Used during and after design entry and before layout, the new tool generates reports that help select optimum test points for in-circuit and functional cluster testing. The package then automatically inserts the test points into the schematic for graphical display and eventual physical test-point analysis and placement.

The other product, "Physical Test Manager: SITE," integrates physical access and test-fixture requirements with circuit design rules and clearances to automatically optimize test-site location. The package achieves high completion rates by using algorithms that support trace shove-aside, test via substitution, stub length control, and true clearance (gridless) positioning. The tool supports in-circuit, cluster, built-in self-test, and scan-test strategies.

Virtual Test Manager: TOP is an option to Design Architect and costs $18,000. Physical Test Manager: SITE, which is an option to Board Station, Board Station 500, MCM Station, or any Mentor pc-board or MCM layout product, costs $20,000. Both will be available in December.

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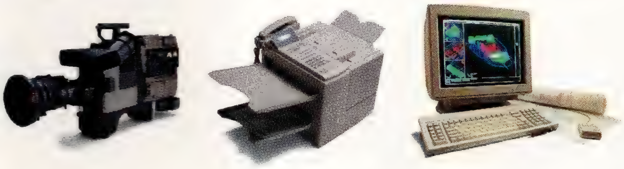

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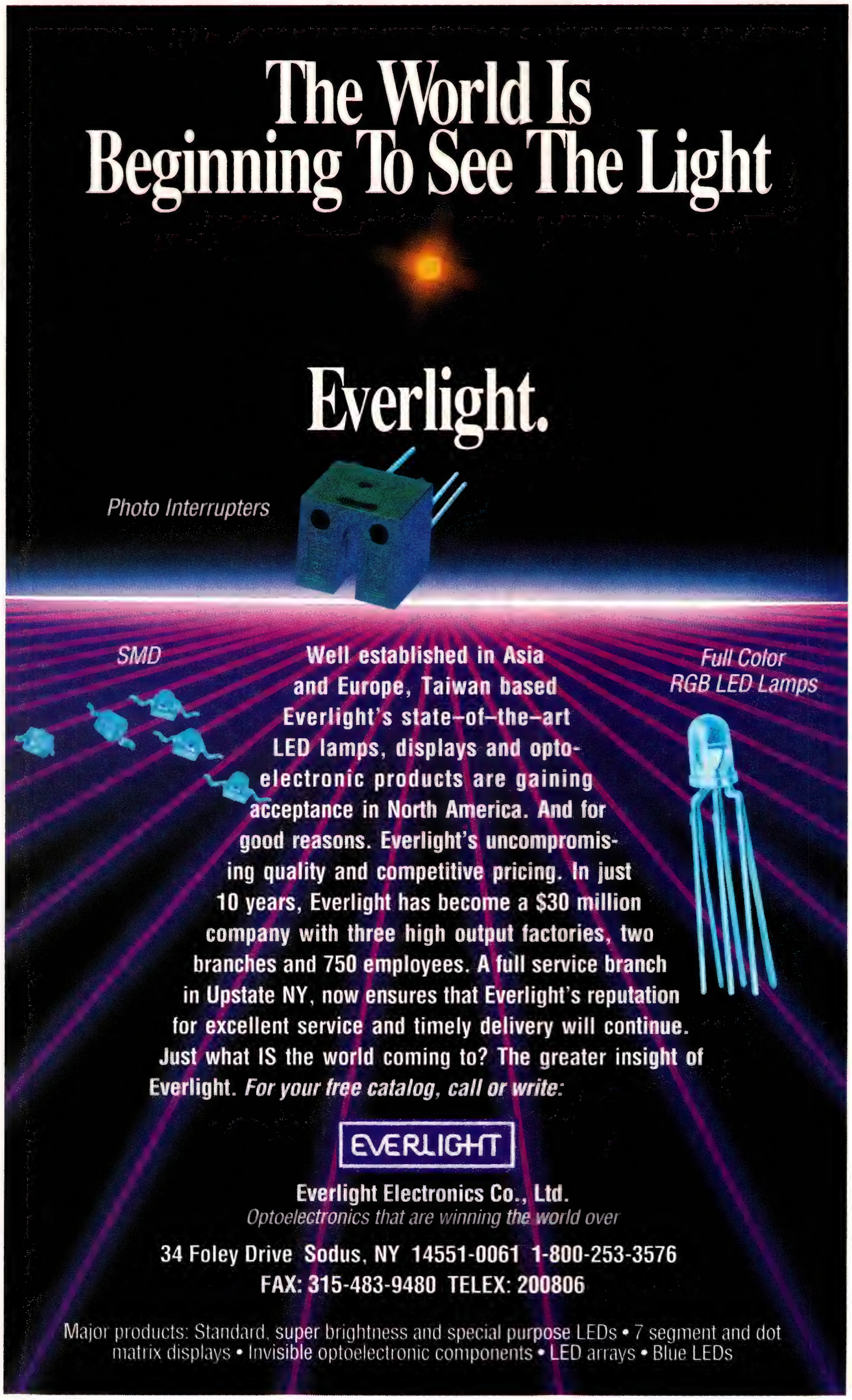

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The testing was complicated by the fact that the device is packaged "cavity-down"—that is, with the die bonded to the package ceiling rather than the floor. This method provides a better thermal pathway to the heat sink above the package, and is being used more often for medium- to high-power ICs and MCMs, says Sekulic.

Designers must plan ahead to ensure successful probing. Sekulic notes that key decisions include the types of tests that must be made, the number of internal nodes to be probed simultaneously, the placement and size of test points on the die, the use of passivation layers, and the need to insert and remove parts from the fixturing. Fixturing will place the device upside down, so the designer must ensure adequate cooling during testing. Sekulic points out that contact probers offer an optional laser to cut an access hole through layers covering the die.

The arrangement used by IMS included a ZIF socket mounted below the contact prober's socket card. A hole was cut in the socket to allow access to the IC *(Fig. 2)*. Initially, probe-tip vibration was a problem when the probe moved from one test point to another. That was solved with a probe tip specifically designed to dampen vibration.

Sekulic notes that direct solder connections are the best, but they make it hard to replace devices. Pin sockets allow easy insertion, but may make it difficult to remove large-pin-count devices. ZIF sockets are simplest, but their height places the die further away from the high-power microscope needed for probe placement, which may cause focus problems. To use a 100X objective lens, a low-profile ZIF socket or an alternative connection method is needed. In IMS' application, the ZIF socket was thin enough to allow 50X viewing of most of the IC. And only 10X magnification was needed to probe bond pads near the edge, where no probe tip interfered with the longer lenses. ☐

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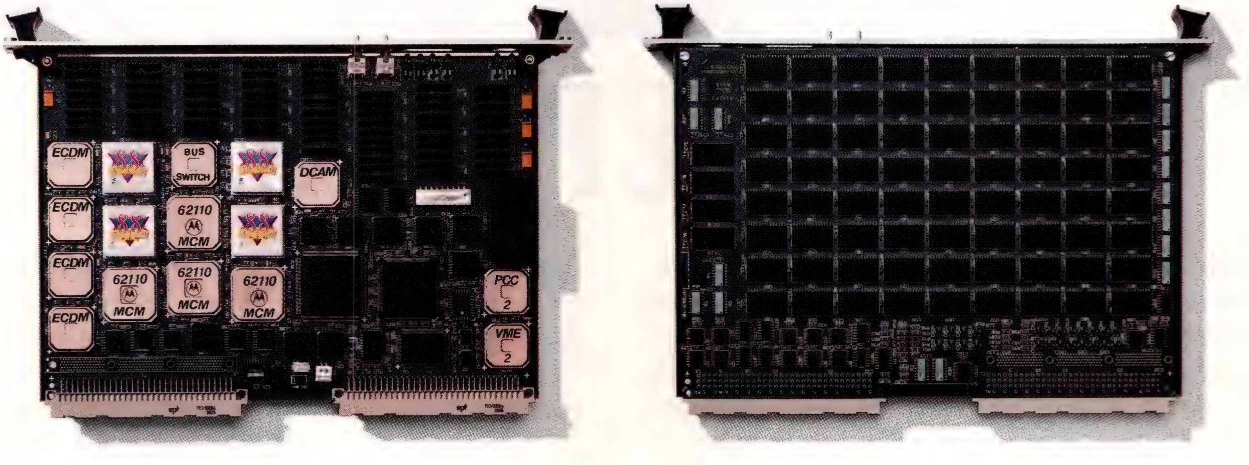

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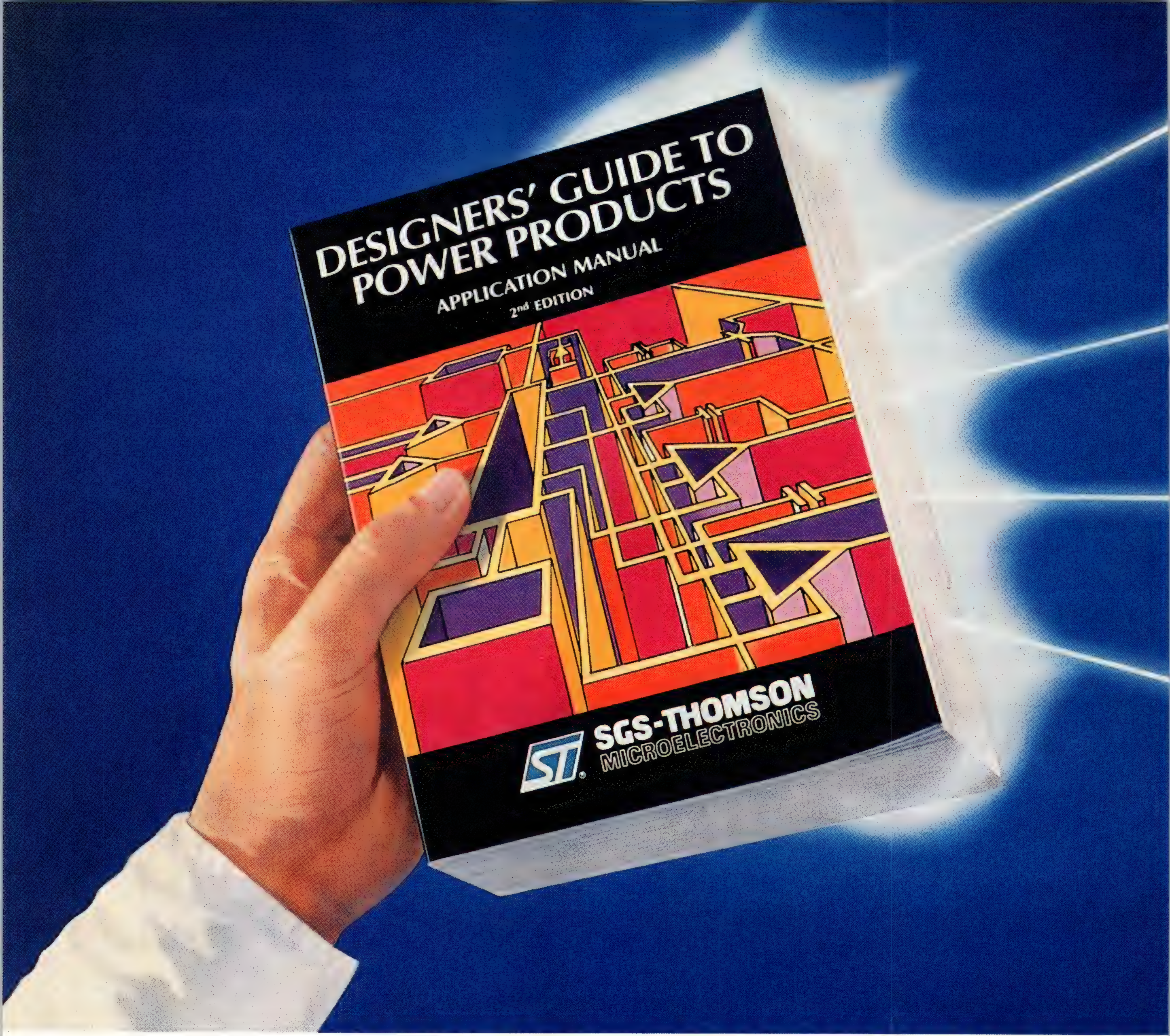

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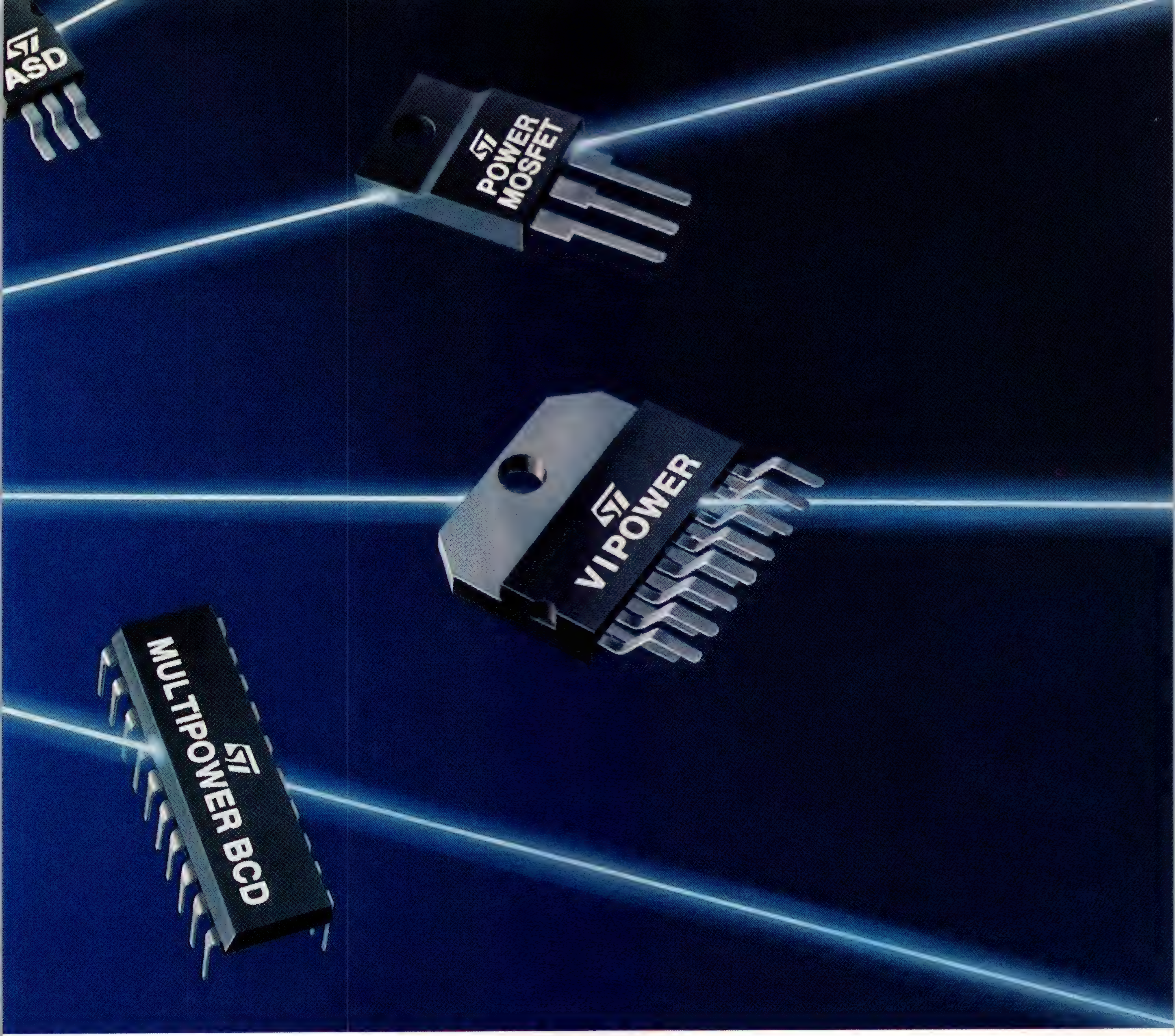

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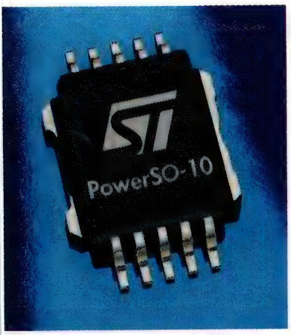

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DIGITAL-SIGNAL PROCESSING GETS READY FOR MULTIMEDIA

FAST KERNELS, A NEW DRIVE TOWARDS STANDARDS AND MULTIMEDIA FUNCTION LIBRARIES PAVE THE WAY.

JACK SHANDLE

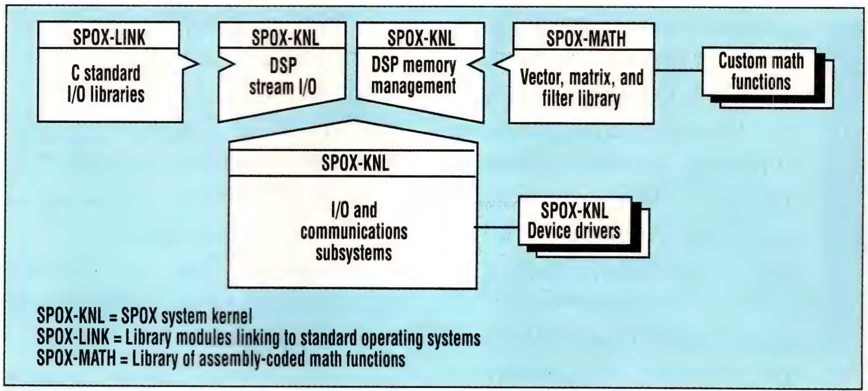
Two of the primary problems holding back the growth of multimedia—useful multimedia standards and multimedia's high computational demands—are merging into a common challenge: To create a cross-platform, cross-processor standard for digital-signal-processing applications.

DSP ICs are viewed in many quarters as a promising solution to multimedia's computational demands for two reasons. First, their architecture is very efficient in executing the plethora of compression, digital-audio, and telephony algorithms that have become part and parcel of multimedia. Second, the chips themselves are relatively inexpensive.

What's not quite as clear-cut is how a common standard can be worked out so that independent software developers won't have to pick and choose between hardware or operating-system software platforms. Contrary to the Intel-dominated world of PC microprocessors, there are at least four important DSP IC vendors: Analog Devices, AT&T Microelectronics, Motorola, and Texas Instruments.

It's probable that the multimedia DSP standard will be software, either in the form of a DSP operating system or a common application programming interface (API). Intermetrics Inc., Cambridge, Mass., is offering still another solution. It's creating a set of DSP development tools that will work with any of the major DSP chip architectures.

Several solutions of a more or less proprietary nature have been proposed. Spectron Microsystems Inc., Santa Barbara, Calif., has revised its SPOX DSP operating system to be friendlier to multimedia. AT&T Microelectronics, Berkeley Heights, N.J., has done the same with its VCOS operating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Voltage Options (V)	2.5, 4.096, 5.0, 8.192, 10.0	2.5	2.5, 4.096, 5.0, 10.0	Adjustable, 1.2
Tempco (max)	100ppm/°C, 150ppm/°C	30ppm/°C (typ)	25ppm/°C	100ppm/°C, 150ppm/°C
Packages	SOT-23, SO-8, TO-92	SOT-23	TO-92	SOT-23, SO-8, TO-92
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system. IBM Corp. and Texas Instruments Inc. have teamed up on a hardware/software architecture called MWave, and Analog Devices Inc., Norwood, Mass., has its Signal Computing Architecture.

Despite claims of openness, it's likely that each of these solutions is aiming at a more or less de facto standard. The Interactive Multimedia Association (IMA), on the other hand, is discussing a cross-platform, cross-DSP API that would allow the multimedia industry to march quickly forward without crowning another set of chip and operating-system kings. Composed of more than 250 companies with a common interest in having multimedia grow quickly, the IMA tries to strike a balance between de facto standards and ANSI-like collaborative standards that often take years to complete. It's doing this across a wide range of multimedia issues *(see "Standards: Multimedia needs to move quickly and competently," below)*. By the time this article is in print, its special interest group on DSP ICs will have met at the DSPx Conference on October 6, San Jose, Calif., to continue discussions on the API.

Although the standards work is promising, the industry can, in the meantime, expect to see fierce competition among both the DSP chip solutions and operating systems.

Sometime before the end of the year, Spectron Microsystems Inc. will release a multimedia development kit based on the most recent version of its SPOX operating system, SPOX 2.0. Kits will be available for Texas Instruments, Analog Devices, and Motorola DSP ICs. The kits will deliver DSP system software that can handle the high-throughput, concurrent-application requirement of PC-based multimedia. They will also offer a set of standard Windows libraries that will shield multimedia applications from the details of DSP hardware.

Among other things, the new SPOX was crafted with a very small and very fast multitasking kernel, says Nancy Haydt, Spectron's vice

STANDARDS: MULTIMEDIA NEEDS TO MOVE QUICKLY AND COMPETENTLY

Most people agree that standards are important and provide comfort and safety to those making investments in high technology. But standards are created in widely different ways and aren't always as stable or solid as we would like to think.

A standard should establish a basis for comparison and assure consistency of parts, components, or data. But just because someone says they have created a standard doesn't necessarily make it so.

Standards always represent some form of consensus, and how consensus is reached determines the standard's strength and stability. Among the most durable and widely recognized are those from bodies such as the International Standards Organization (ISO) or the American National Standards Institute (ANSI). These organizations have established procedures which virtually guarantee that proposals are open and technically complete, and have gone through international review and approval.

The good news is that formal standards are usually quite durable. The bad news is that they can take many years to finalize—ISO standards commonly take six or more years to be finalized. In the world of computers and multimedia, technology changes dramatically during that time. That's why many high-technology executives no longer pay much attention to formal standards organizations.

At the opposite extreme are de facto standards, where consensus is passively observed. If millions of people elect to purchase a particular technology-based product, that constitutes a powerful consensus. One might speculate about the actual basis for an individual's purchase decisions (e.g., effective advertising, market dominance, technical merit, etc.), but the mere existence of a large homogeneous installed base of technology is sufficient to define a standard.

Many high-technology marketing executives, particularly within the personal-computer market, think de facto standards are the only kind that are relevant. Many believe that no valuable work is ever accomplished in committee, which is the way formal standards bodies are allowed to operate (it's not surprising that those who criticize committee standards efforts tend to work for companies in relatively strong market positions, whereas smaller organizations and end-user communities usually prefer open standards efforts).

In the opposing camp, a "proprietary standard" is considered a contradiction of terms. It turns out that proprietary standards can work provided they're administered in a fair and legal fashion and aren't used to promote anticompetitive activities. Usually this means establishing reasonable licensing options that are available to everyone on an equal basis (e.g., compact disc standards by Philips and Sony).

Nonetheless, there are many times when a vacuum in the market forms the need for standards before the market establishes de facto standards. But, in a technological arena that moves quickly, formal standards bodies aren't much help. Here's where a third kind of organization, placed between the rival standards camps, can rise to the occasion.

The Federal government established trade associations as one of the few safe ways that directly competing corporations may legally and reliably collaborate and develop common representation. Corporations who meet under an association umbrella generally do so to directly benefit their industry—as a whole. Associations have often been spawning grounds for major standards agreements, many of which graduate to more formal standards bodies once supported and adopt-president of marketing. SPOX had previously been known as an all-encompassing, 32-bit operating system, but "we found out that engineers were more likely to use 16-bit DSP ICs in their multimedia applications, or 24-bit DSP ICs if they were using Motorola devices," she says.

The main components of the SPOX 2.0 architecture are the operating-system kernel called SPOX-KNL, an array of functions called SPOX-LINK that communicates with the host, and a library of mathematical functions called SPOX-MATH *(see the figure)*.

SPOX-KNL is a real-time, multitasking kernel that can use as little as 1.5 kwords of code space. It can handle preemptive, event-driven scheduling of multiple prioritized tasks and includes a comprehensive set of system services. Among them are memory management, hardware interrupt-handling facilities, control of multiple real-time tasks, and a uniform device-independent interface to I/O and communications.

ed by key industry leaders.

This is the venue used by the Interactive Multimedia Association to foster cross-platform compatibility for multimedia products. About one year ago, the IMA's steering committee approved the Digital Audio recommendation. At Fall Comdex '92, Analog Devices, Motorola, and AT&T Microelectronics demonstrated DSP chips that support these audio formats. In addition, Microsoft will incorporate the formats as a registered data type.

Many more initiatives are underway. In December 1992, the IMA issued requests for technology in three critical areas: Multimedia Data Exchange; Multimedia System Services; and a Scripting Language for Multimedia Portability. We've received good responses, but more work in other areas remains to be done.

Written by Philip V. W. Dodds, the executive director of the Interactive Multimedia Association. Headquartered at 3 Church Circle, Suite 800, Annapolis, Md. 21401-1933, it consists of more than 250 corporations, including Apple, DEC, Hewlett-Packard, IBM, Intel, Kodak, Lotus Development, Microsoft, Pioneer, and Sun Microsystems.

SPOX-LINK comes in three flavors to support common operating systems: DOS, OS-9, and VxWorks for Sun workstations. In each instance, SPOX-LINK provides host-based file I/O, DSP C compiler extensions, formatted I/O, and host-utility functions. SPOX-LINK for DOS, for example, is composed of DSP API and DSP runtime modules as well as DOS API and DOS runtime modules. Although Spectron is expected to provide multimedia development kits supporting TI, Motorola, and Analog Devices DSP ICs, the fourth chipmaker, AT&T Microelectronics, has its own OS.

MWAVE TARGETS ISVs

The joint IBM-TI initiative called MWave, combines two new DSPs from TI with a IBM software. The TMS320M500 and M520 are 16-point, integer DSPs targeted at the PC environment by integrating functions such as an ISA interface and UART capability. MWave software includes a small, deterministic kernel, software that runs on the host PC's processor to manage the DSP, and devices drivers.

MWave's goal is to provide a structure for DSP systems that is open enough to be attractive to independent software developers, says Glenn Sheldon, program manager for IBM's MWave Systems Group, Raleigh, N.C. The MWave Manager creates a direct link between the microprocessor operating system and the DSP, and the MWave kernel is robust enough to handle the hard real-time requirements of multimedia functions that need service data at specific rates.

For the time being, MWave's future is in providing resources to a coprocessor DSP, but in the future IBM may repurpose the software to a different role. Fred Sporck, IBM's program manager for the PowerPC microprocessor, has indicated the new RISC engine has enough mips to handle the algorithms that typically call for a DSP.

But mips are not enough. An operating system kernel capable of handling the real time demands of multimedia would also be in the cards. Unless there is a hard real-time OS to service the interrupts, then there is no guarantee that there would not be breakups in speech, for example, says Sheldon. Although one might want the main processor to do some low-level operations, it would be prudent to include a DSP in the mix.

VCOS ENABLES TELEPHONY

VCOS Version 1.1 was announced in August. It provides several new features, including a resource manager for allocating multimedia applications across multiple DSP ICs, power management for computer-based telephony, and modem/fax software libraries. The resource manager allocates the computing resources of multiple DSP ICs among tasks and I/O devices, such as speakers, microphones, and telephone lines. It also provides load balancing across chips and applications.

One of the key attributes of VCOS is its ability to share memory with the host. That's because a major cost hurdle of using DSP ICs as coprocessors isn't the cost of the DSP chip itself, but rather the "redundant" memory it requires. Using system memory raises difficult issues, however, such as relative access times. Typical host PCs have average access times of 200 ns for block moves and more for individual memory accesses. DSP ICs, on the other hand, require access times of 20 to 45 ns. So even if a DSP algorithm could be executed from host memory, the many bus requests would impair system performance.

To solve this problem, VCOS operates on frames of data rather making a memory access each time it needs one. Because each frame has a known number of samples, the DSP IC accesses memory in blocks rather than with random individual memory accesses. The real-time execution is performed within the DSP device and its internal memory. AT&T calls this technique a visible caching strategy because the DSP algorithm developer—not the hardwired on-chip logic—determines what gets cached. The host processor can operate in parallel with the full resources of the PC bus at its disposal.

To develop multimedia applications on VCOS, the VCOS Application Server and the VCOS multimedia library come into play. VCOS is accessed through such tools as Microsoft's C and Windows development kits rather than specialized DSP tools. The multimedia module library consists of algorithms developed at AT&T Bell Laboratories, although algorithms from other sources can also be used.

SIGNAL COMPUTING

Analog Devices' Signal Computing Architecture takes still a different approach. Although it includes a business model that involves chip and algorithm developers cooperating on specific reference designs, its open-architecture component is software-based.

It proposes a seven-layer software model that's analogous in concept to the OSI telecommunications model. The upper four layers reside on the PC and its microprocessor. The top layer is the user interface and below that is the application-program layer. The third layer, which is called the API layer, is where the application program's needs are translated into specific instructions and system-services requests. Layer 4 is the PC's operating system, which provides coarse timing, prioritization, synchronization, and scheduling among the applications requesting service.

The lower three layers are embodied in the DSP chip set and algorithm. Layer 5, the algorithm layer, defines how the specific application needs will be implemented in real time. Layer 6 the DSP operating system, and the layer 7, called the language layer, provides the instructions for the DSP circuit as executable code.

Clearly, the technology directions espoused by IBM, Spectron, AT&T, and Analog Devices aren't entirely exclusive of each other. In fact, the API developed as part of the IMA's standards-making initiatives might well work with them all. One thing is clear about the coming convergence of DSP architectures, however: Software will play the major integrating role. No one expects to see a rerun of the microprocessor shoot-out that ended in Intel's dominance.

"People are not going to get sucked into a specific hardware architecture," says Satish Gupta, vice president of Media Vision Inc., a leading multimedia systems company. "The real standards are Windows, QuickTime, and OS/2. Anything that succeeds is going to have work with them."☐

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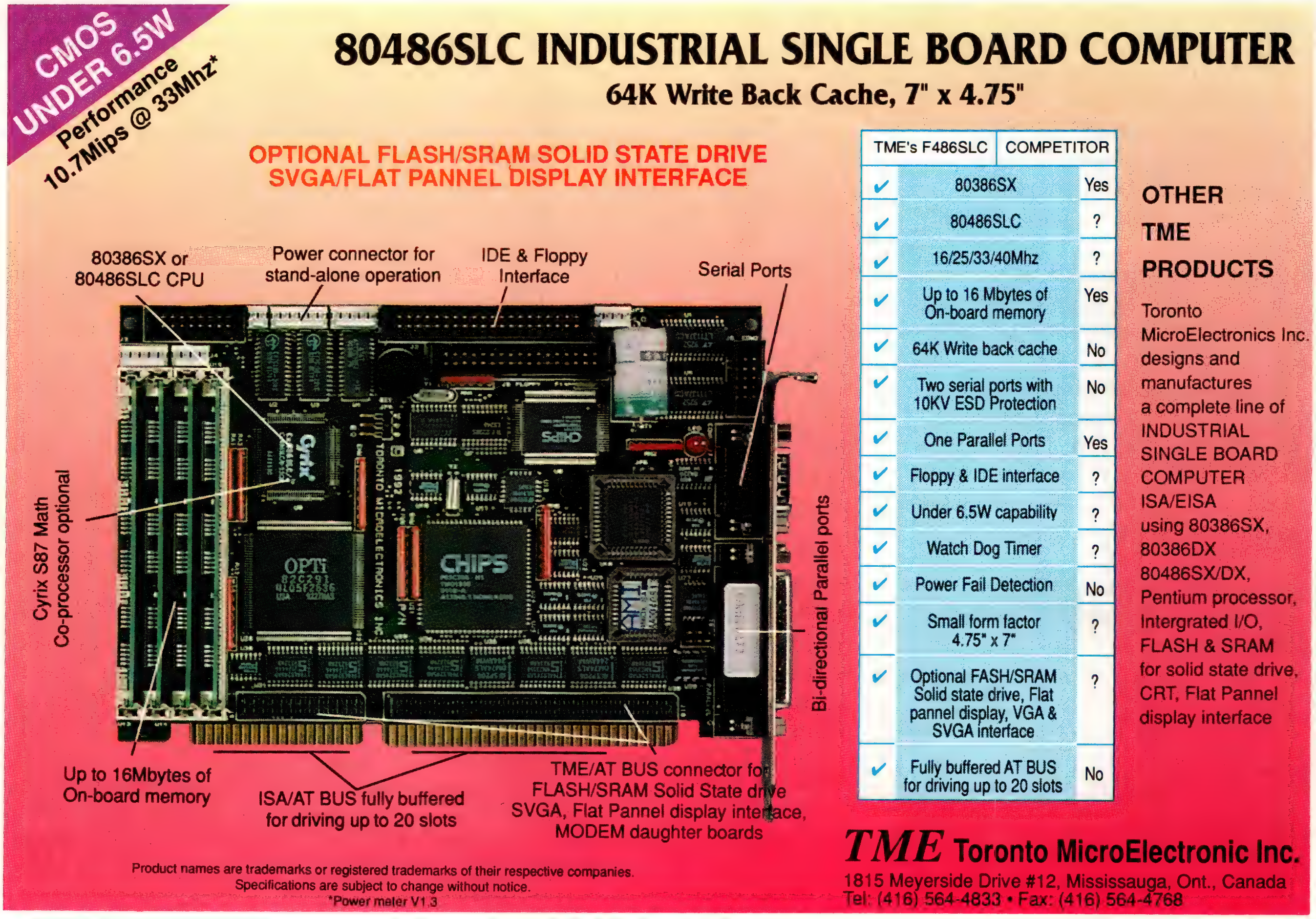

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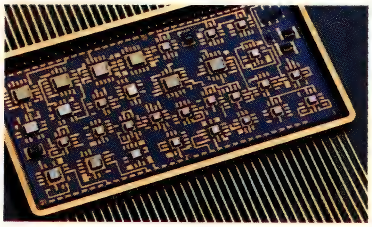

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MICROCONTROLLER SWITCHES 5-A, 60-V CURRENT PULSES

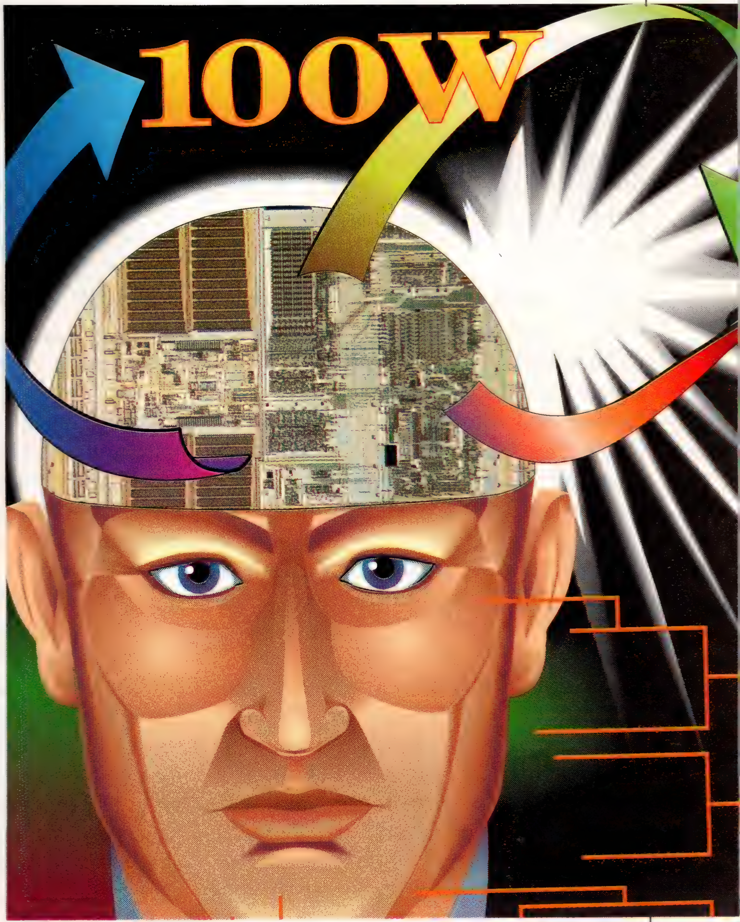
FRANK GOODENOUGH

During the past dozen or so years, there's been a parade of so-called "Smart Power" technologies along with the numerous ICs built on them. The ICs range from linear and switching regulators to digitally programmable motor controllers. In some cases, the "smarts" were analog, in some cases digital, and in other instances the two were blended. Versatility was limited, though, since they were aimed at very few applications—often just one.

SGS-Thomson Microelectronics has come up with a true "Smart Power" technology: It's the first IC that can be used for general-purpose applications. SGS's designers added a 60-V DMOS FET H-bridge, which can be operated as a pair of independent half bridges, to the company's ST6 8-bit microcontroller. Each of the four FETs forming the bridge carries a continuous-current rating of 1 A. It can handle non-repetitive peak-current pulses (less than 50-µs long) of 5 A and continuous peak-current pulses of 3 A. On-resistance of the four power FETs runs 300 mΩ.

SGS dubbed the technology BCD3; its first IC is the H081. BCD3 represents a third generation of their multipower bipolar, CMOS, DMOS process technology with line widths reduced to 1.2 µm *(see "BCD process evolution," p. 77)*. The circuit density provided by this fine-line process makes it economically feasible to integrate the ST6 and peripheral circuits on a chip with one or more power MOSFETs, their drive circuitry, and analog support circuits *(Fig. 1)*.

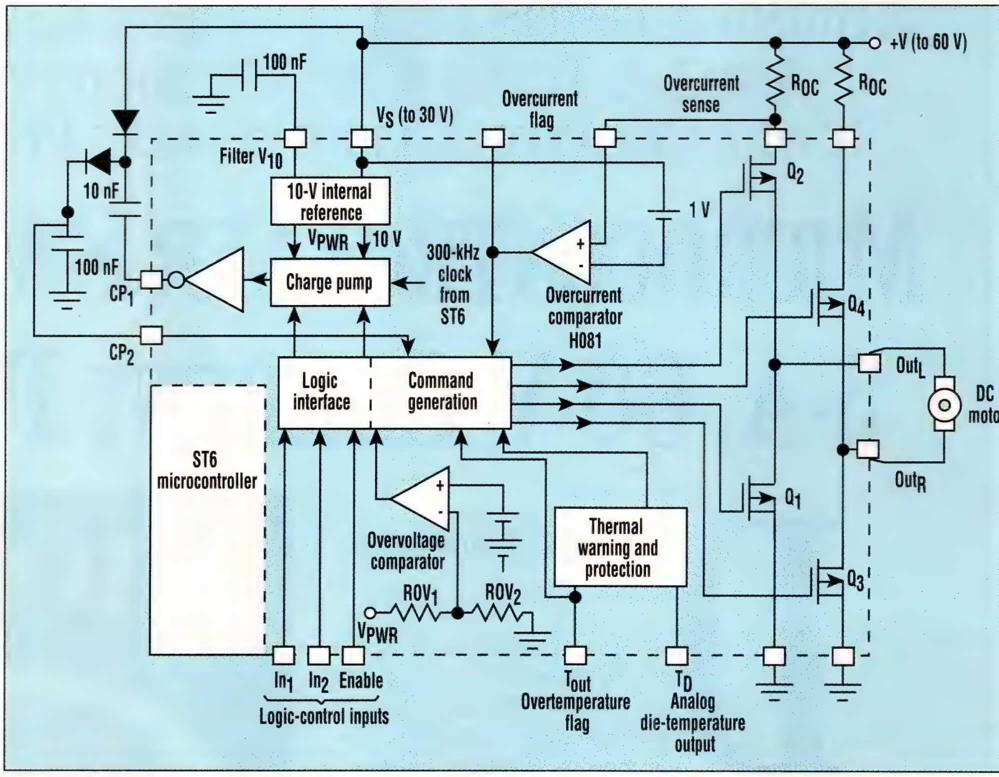
The BCD3 technology's capability can be seen in the H081. The IC is designed to drive bidirectional dc motors, but its output can be configured and controlled as a pair of half-bridges driving two separate loads. The BCD3 process also offers the possibility of putting an EEPROM on the H081 for additional system flexibility.



The technology not only makes possible complete control systems on a chip, but a system designer can also trim time-to-market by creating a chip before the system design is fully defined. As the system is developed and debugged, the chip's functionality and characteristics can be changed simply by modifying the software.

Adding an EEPROM can create power-control ICs that adapt to changing conditions. For example, a motor driver can modify its control strategy as the motor and other system elements age to maintain optimum performance. EEPROM-based chips also lend themselves to multichannel systems in which one serial bus carries the control signals for a number of widely dispersed load controllers, each with its own microcontroller. On-chip EEPROM can also adjust circuit and system gain, zero offsets, adjust references, and add product-code IDs at any time after manufacture.

A technology like BCD3 challenges the imagination of system designers and marketeers alike. For example, it could form the heart of a one-chip active noise canceller for air conditioners, range-top hoods, and other noisy appliances. The process integrates a microphone preamplifier, an analog-to-digital converter (ADC), a DSP core, an output digital-to-analog converter (DAC), and a DMOS audio power amplifier already available on a higher-voltage 100-V BCD process (ELECTRONIC DESIGN, *June 11, 1992, p. 67)*.



1. THIS TRUE "SMART POWER" IC contains an 8-bit microcontroller, a 60-V DMOS FET H-bridge rated at a continuous current of 1 A, and an assemblage of control, drive, and protection circuits for the bridge and its load. The H081 was developed by SGS-Thomson.

Though a noise canceller represents a special application, the process could also create a family of general-purpose drivers. These ICs would include a core microcontroller, interface I/O, EEPROM, and a number of uncommitted DMOS power FETs. Loading suitable software can at any time set the configuration and performance of the output devices. Analogous to PLDs, these devices could significantly simplify the design of power circuits. In addition, system houses would only have to stock one standard device for use in many products.

The technology could also be used to build a general-purpose, programmable, single-chip power supply to replace dozens of different types of supply chips now in use. Such a chip gives power-supply engineers a chance to change designs in minutes just by altering a program. The IC could integrate a microcontroller core, memory, a serial interface, various analog and digital glue circuits, and several uncommitted power FETs. A power supply's basic topology and/or operating modes would be set in software or even adjusted in the final application by loading commands via the serial bus. If allied with a host microprocessor, dialogues between it and the power-supply chip's controller can implement complex energy-control strategies.

Here's how the H081 works *(Fig. 1, again)*. Pulse-width-modulated (PWM) control signals from the ST6 microcontroller feed the logic control inputs. The logic-interface and command-generation circuitry convert the logic signals to the 10-V pulses required to turn on the low-side FETs, Q_1 and Q_2. And, with the help of the charge pump, the drive for high-side FETs Q_2 and Q_4 is brought to 10 V above the power-supply rail (V_S) to turn them on. The chip's suite of self-protection circuits handles overvoltage, overtemperature, overcurrent, and undervoltage conditions, and guarantees that all four power FETs are off when the ST6 is in a reset mode.

The ST6 microcontroller is completely independent of the chip's analog/power-control circuits. The two sections of the chip each have their own control, data, I/O, and power-supply pins for maximum system flexibility. The ST6 consists of six major blocks: a 64-byte program RAM, a timer, a watchdog circuit, a clock/oscillator, a serial I/O port, and a CPU/interrupt controller. Although the microcontroller has no ROM, it can still be employed in many power-control applications, and as

TRUTH TABLE FOR POWER-FET CONTROL

Enable	In$_1$	Out$_R$	Enable	In$_2$	Out$_L$
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0	1	H	0	1	H
0	0	L	0	0	L

X = don't care Z = high impedance

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noted, EEPROM or other memory can be added to future or custom versions of the H081. The microcontroller section runs off a single 5-V power-supply rail.

HIGH/LOW VOLTAGE

Putting 60-V power-supply rails on chips that also carry an abundance of 5-V digital and 10-V analog circuits demands much of a layout designer's skills. The H081 is no exception. While both its analog and digital circuits are relatively straightforward, layout of the H081 required several tricks to minimize the effects of bipolar parasitic devices when they turn on *(Fig. 2)*. The major parasitic effect occurs when one of the outputs goes below ground level, such as when turning off an inductive load. At that time, the source-drain diode in the low-side FET switches on, as does the device's parasitic npn transistor, which can sink current from any epitaxial pocket in the chip.

To avoid this effect, the two low-side FETs are located at the chip's corners and the microcontroller is located as far as possible from them. In addition, each low-side FET is surrounded by a protection ring called the Maginot Line, which is composed of several proprietary diffusions. For further protection, a second Maginot Line crosses the die, separating the analog and power circuits from the microprocessor.

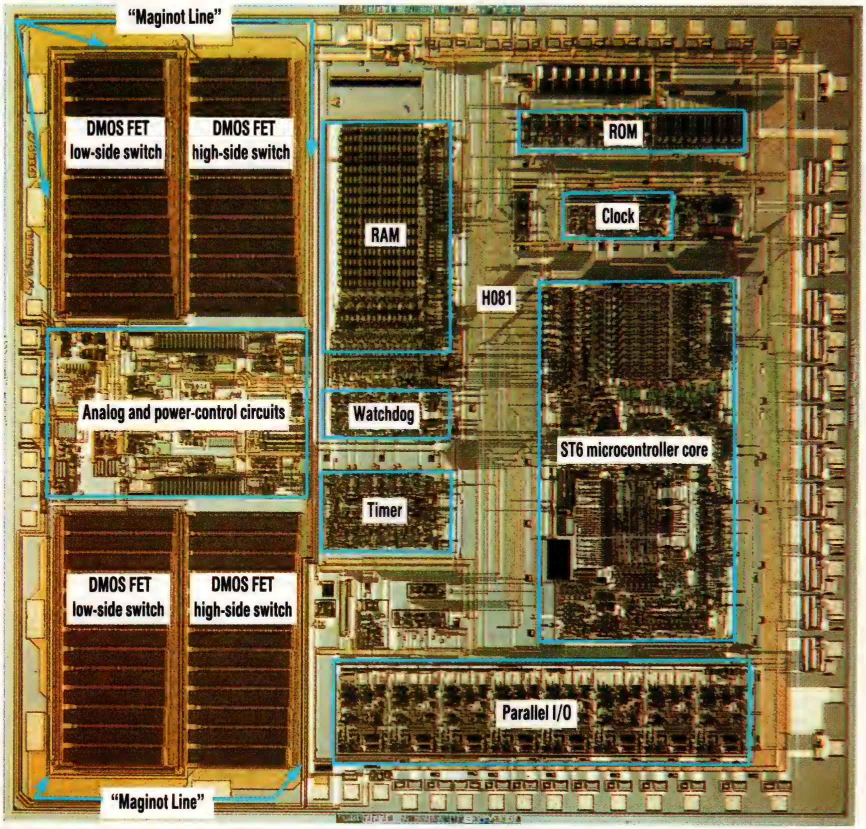
The H081 is packaged in a 68-pin PLCC. The high pin count is necessary to provide I/Os for addresses, an external data ROM (24 pins), and to keep the two sections of the IC independent of each other. The independence also simplifies testing since the ST6 and the analog/power section can be tested separately. Only one signal, a 300-kHz clock from the ST6's clock prescaler to the charge pump, is routed on-chip between the two sections.

Because the ST6 has a serial I/O, operational speed is low. Each ST6 operational cycle needs 13 clock periods to completely shift the program counter. Therefore, it takes 6.5 µs to load instructions. However, the ST6 offers block modularity, which means that other blocks can be incorporated simply by adding decoders to the CPU. For example, because the 1-bit ALU operates serially, a fully parallel architecture can be imhad with an 8-bit parallel ALU.

The ST6's 64-byte RAM is big enough to provide read/write operations for internal variables during computation. Typical jobs handled by the timer include generating a PWM signal, calculating delay, or determining the frequency of the input signal.

The watchdog circuit, also a timer, counts backwards and generates a reset signal when it "times out." In a noisy application, it controls the flow of program instructions. If, for example, program flow changes because of external events (such as noise spikes), the watchdog timer resets the entire chip and restarts the program. The on-chip clock operates with an external resistor or crystal (a metal-mask option). It can be stopped to decrease power drain.

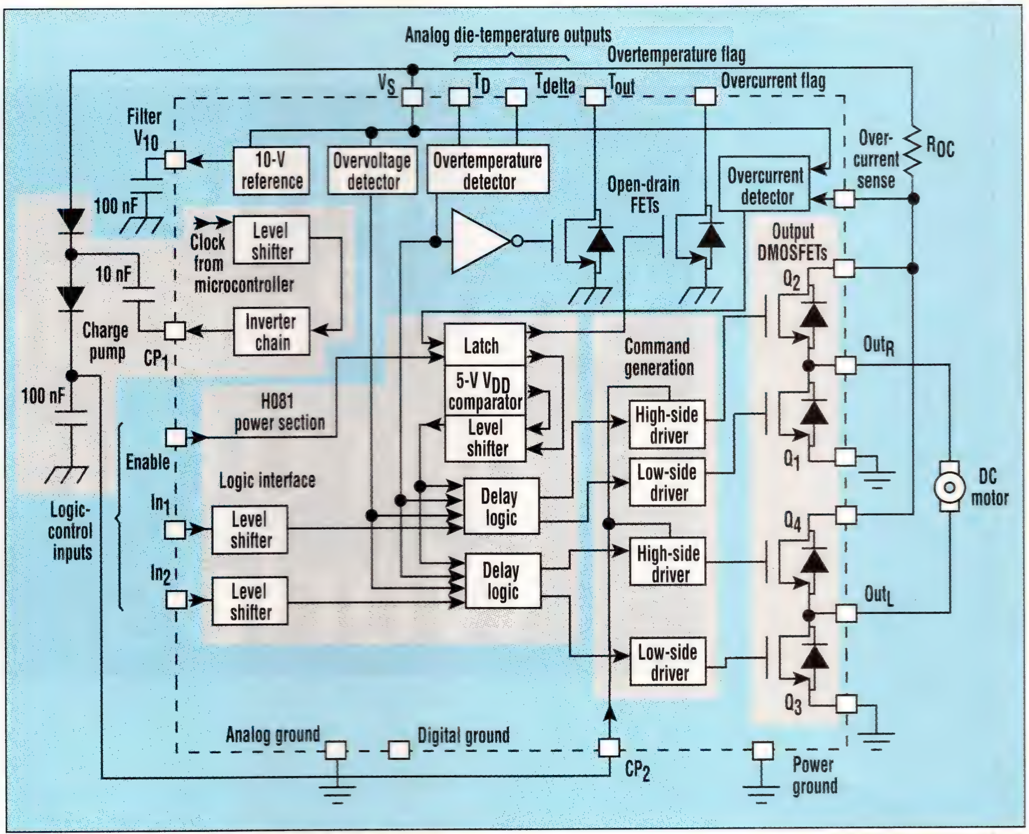
The CPU core of the ST6 controls the other blocks. It translates the input opcode coming from the external ROM. The core contains a PLA and a simple phase generator that creates 13 separate phases, which in turn limit the controller's speed (additional information on the readily available ST6 can be obtained from SGS-Thomson).



2. TO "SAFELY" PUT 60-V DMOS FETs on a chip with a 5-V microcontroller (the SGS-Thomson ST6) and 10-V analog circuits, the low-side power MOSFETs are placed on the corners of the chip that are as far as possible from the ST6. In addition, a "Maginot Line" formed with two diffusions was inserted around both low-side FETs. A second such line was placed between the 5-V logic circuits and the analog and power-control circuits.

H081 BLOCKS

The analog/power-control section of the H081 consists of six major blocks: a logic-interface section, a command-generation section, output MOSFETs, a charge pump, protection circuitry, and a voltage reference *(Fig. 3)*. The IC requires two external positive power-supply rails. The main supply rail, V_S, is typically about 14 V. The control-logic supply voltage for the analog section, CV_{DD}, should be 5 V (the same as the power-supply rail for the ST6). CV_{DD} should come from an external regulator because it's used as both a reference voltage and as the supply voltage for the Schmitt triggers on the control-logic inputs Enable, In$_1$, and In$_2$. If a supply voltage greater than 30 V is connected to the drains of the high-side MOSFETs, they and V$_S$ must run off separate power supplies. That's due to the overvoltage detector shutting down the outputs once V$_S$ exceeds 31 V.



3. THE POWER SECTION of the H081 takes 5-V logic-control signals from the on-chip microcontroller and level-shifts them to 10-V signals. Thus, it boosts the gate drive for the two high-side power FETs to 10 V above the power-supply rail connected to their drain.

The analog section has a third supply-rail input, CP$_2$—the output of the charge pump that develops the voltage. It's approximately 10 V higher than V$_S$ (24 V if V$_S$ = 14 V) and is needed to drive the gates of the high-side FETs. If an external voltage 10 V greater than V$_S$ is available, the charge pump that's driven by the controller's clock isn't needed. For example, during system development and/or testing, using an external power supply permits shutting down the microcontroller while maintaining the analog circuitry's functionality. Much of the circuitry in the analog section of the H081 runs off a 10-V reference whose output is derived from V$_S$. The reference can be sensed and is filtered by an external capacitor.

During normal operation, the four power FETs are controlled by 5-V logic signals on the Enable, In$_1$, and In$_2$ pins *(see the table)*. The two logic-input signals, In$_1$ and In$_2$, and the clock from the ST6, are referenced to the 5-V power-supply rail. When applied to the chip's analog section, it level-shifts them to 10-V pulses referenced to the "Filter" V$_{10}$ pin. The level-shifted clock pulses feed a current (power) amplifying chain of 5 inverters. The output of the 5th inverter connects to the output pin CP$_1$, which drives the external charge-pump circuitry.

The H081's analog section treats the Enable logic-control signal with additional respect, turning it into a general "enabling" pulse for the power FETs. When it's at a logic high (5 V), it calls for a "not-active" mode of operation. All four FETs are switched off and both half-bridge outputs (Out$_R$ and Out$_L$) are in a high-impedance state. When it's at a logic low (0 V), the circuit is in an "active" mode and the outputs are forced to the condition called for by the In$_1$ and In$_2$ inputs, per the truth table.

The decision to have the Enable pin active when in a low logic state represents a function of the interactions between the ST6 and the H-bridge. That is, when the ST6 is being reset, its output ports are fixed high by an internal pull-up resistor. If the Enable pin is "active low," the chip guarantees that all four power FETs are off during the reset mode.

The Enable signal feeds a latch, which also receives an input from the overcurrent comparator *(Figs. 1 and*

BCD PROCESS EVOLUTION

When first introduced in 1986, multipower BCD employed 4-μm geometries and required 14 to 16 mask steps. The process made it possible to integrate multiple, isolated vertical DMOS power transistors. The second generation 2.5-μm BCD2 process required 16 to 18 mask steps. This version doubled signal component density and the power density of the DMOS FETs. It also added double-level/dual-thickness metal and low-leakage diodes. BCD2 has been successful in integrating all of a hard-disk-drive's power circuits.

The third generation BCD3 process couples 1.2-μm-minimum line widths with an alignment tolerance of 0.4 μm. Using 18 masks, it offers all of the features of its recent predecessor plus double polysilicon and double-level triple-thickness metal. BCD3's CMOS FET density is 5000 transistors/mm^2 versus 1600 for BCD2.

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3, again). One latch output feeds the overcurrent warning-flag pin; a second output is level-shifted, becoming a 10-V signal instead of 5 V.

If the analog section doesn't have 5 V on the CV_{DD} pin, all level-shifter inputs will lack a reference. That is, they'll be undefined and any or all of the power FETs may be switched on. To avoid this situation, the V_{DD} comparator looks for 5 V on the line from CV_{DD}. If it's lower than approximately 3 V, the level-shifter output signal will look the same as if the Enable signal were high (non-active) and the power FETs are switched off.

The delay-logic circuits perform the following functions: If the inputs from the overtemperature and overvoltage detectors are inactive (temperature and voltage are within limits) and if the level-shifter output signal is active, the state of logic control inputs In_1 and In_2 are analyzed separately. If either In_1 or In_2 remains a stable low for at least 200 ns, the delay-logic circuit puts out a logic low to its respective low-side driver, which then switches on the respective low-side FET.

In a similar manner, if either In_1 or In_2 remains a stable high for at least 200 ns, the delay-logic output activates its respective high-side driver. A current mirror in the high-side driver, connected to the high voltage from the charge pump at CP_2, charges the gate capacitance of its high-side FET turning it on.

Like most of today's power ICs, the H081 incorporates a suite of self-protection circuits *(Figs. 1 and 3, again).* The overvoltage comparator senses a fraction of V_S attenuated by an internal resistive divider that's formed by ROV_1 and ROV_2. If V_S exceeds 31 V, the overvoltage circuit intervenes and turns off the FET switches. The circuit incorporates 1.2 V of hysteresis. When the die temperature approaches 170°C, the overtemperature detector feeds a shutdown signal to the delay-logic circuits and produces a digital open-drain (active-low) signal at the overtemperature-flag output pin. When shut down, the two outputs are in a high-impedance state. The circuit restarts automatically when the die temperature drops to 140°C, creating 30°C of hysteresis.

An analog output is also available at the T_{delta} pin. It provides a voltage proportional to temperature of about –6 mV/°C. By sensing the die temperature and sending it to an ADC, the microcontroller can create complex protection schemes and reduce power under critical conditions to avoid complete system shutdown. This is extremely valuable during system development and testing.

Overcurrent protection is implemented by sensing the voltage drop across a user-selected external resistor R_{OC} in series with the load. If the voltage at the sense pin exceeds 1 V for more than a few microseconds, the circuit kicks in, latches, and turns off the FETs. Setting the value of R_{OC} establishes the circuit's trip point. A subsequent falling edge on the Enable signal resets the latch and restores operation. Also provided is an overcurrent, open-drain output flag.

WHAT NEXT?

SGS is currently designing a broad family of circuits that can be added onto a BCD3 chip with a microcontroller. These include ADCs to provide feedback of the variables under control to the microcontroller; a hardware watchdog timer that doesn't require the processor's clock; an internal voltage regulator with the potential to power external circuits; a PWM loop; and some form of ROM, probably implemented in EEPROM. In addition, designers may have access to a library of SGS CMOS cells designed for a 1.2-μm process and all ST6, ST7, and ST9 microcomputers.☐

PRICE AND AVAILABILITY

The H081 power IC with an H-bridge and microcontroller comes in a 68-pin PLCC. Rated for operation over the commercial-temperature range, it or similar ICs will sell for approximately $5 to $6 each in OEM quantities, or $10 each in 1000s.

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ANALOG
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CREATING AND MANAGING DESIGN LIBRARIES

As design automation assumes more of the product-development cycle, the need to generate and manage electronic data is crucial to a project's success. Because each CAE or CAD tool operates off a unique set of models and libraries, designers are often overloaded with data in a variety of formats. Consequently, the data-generation and -management problems faced by today's design teams are quickly becoming more important than EDA-tool functionality and performance.

The following three articles address several important issues dealing with EDA libraries. The first article, from Compass Design Automation, outlines how engineers looking to purchase physical libraries for IC design can evaluate their options. Next, an article from Mentor Graphics explains what aspects of physical-library development are key to today's high-end IC designs. Finally, an article from AT&T Bell Laboratories describes the importance of a component-data-management system to the quality of an end product when doing complex system design.

USER-DEFINED BENCHMARKS HELP EVALUATE IC PHYSICAL LIBRARIES

PERFORMANCE, AREA, FUNCTIONALITY, AND FLEXIBILITY DETERMINE THE BEST SOLUTION.

BY HARRIET HARVEY-HORN
Compass Design Automation

Unlike the past, in which libraries were only provided by ASIC vendors or developed by internal development groups, a number of options for setting up IC libraries now are available. For instance, out-sourcing of physical-library development has recently become a new alternative for integrated-circuit design teams. However, evaluating the commercial libraries to determine their suitability for specific design needs presents quite a challenge.

Because purchasing physical libraries is foreign to designers, no standards exist for their evaluation. The situation is further complicated by a broadening definition of the term "library," which refers to traditional behavioral and logical libraries as well as physical-layout libraries. Determining what exactly is being provided in a library solution and how well the solution meets the user's needs for functionality, performance, area consumption, and flexibility are key to an effective library-selection process.

Assessment of any IC-development capability must begin with an understanding of the designer's needs *(Table 1)*. In the specific case of libraries, the priority of these needs depends upon the type of design style or market segment the end product will address. IC and ASIC designers, whose primary objectives are delivering the most competitive new designs as quickly as possible, require not only the densest, best-performing solution possible, but also the ability to use the libraries with today's design tools.

Library-development engineers work to provide IC designers with the means to achieve their density, performance, and productivity objectives. The library developer's problem is complicated by the fact that varied end-user applications and design environments require a flexible and broad library solution. This solution must include a broad set of functional libraries, interfaces between those libraries and multiple EDA environments, and a prompt response to new generations of process technology.

To understand the benefits of a library solution, it's important to know the library's attributes and which of those attributes has the greatest impact on design objectives. An overly simplistic assessment of features such as the size and performance of basic gates will provide a measure of individual cell size and performance, but won't reveal chip-level capabilities or designer productivity. Likewise, an overly constrained and multidimensional evaluation is informative, but can prove time-consuming and may obscure the significant results of the evaluation. Basic knowledge of architectural features and library-generation techniques offers valuable insight for library evaluation.

Many architectural trade-offs are

TABLE 1: PRIORITY OF LIBRARY ATTRIBUTES

	Size	Performance	Functional breadth	Ability to customize	Links to EDA tools	Process portability
Library developer	High	High	High	Medium	Medium	High
Full-custom designer	High	High	Medium	High	High	High
Systems designer	High	High	Medium	Medium	High	Medium

associated with a given library. First, the porosity of library elements (the design of individual elements such that routing blockages are minimized) may result in slightly larger elements, but will provide denser results at both the block and chip level.

Drive strength and buffering can also be addressed in various architectural ways. The trend is for libraries to be designed with minimum transistor sizes and minimal buffering, allowing synthesis tools to add buffers and drivers as needed. While this approach can achieve impressive results in gate or transistor density, overall block area must not be overlooked. For instance, a library architecture that has unique library elements designed with high-drive transistors or optimized buffers may provide a block-level area advantage, particularly for designs with more demanding performance or drive requirements *(Table 2)*.

Finally, block generators or compilers may offer an advantage over fixed configurations. For components such as memory, multipliers, and datapaths, the ability to compile a configuration for a given application yields a productive and optimized implementation.

Library-generation techniques have a great bearing on the library's flexibility and utility. A significant aspect of the generation process is its adaptability to new or different process technologies. A library solution that takes six months to target to a new technology may not address the needs of designers who must rapidly access the latest IC process. On the other hand, a library that can be retargeted overnight using hard-coded algorithms may lack the functional breadth and/or flexibility required for various design applications.

Another aspect of library generation is the varying degrees of linkage it provides to EDA tools. This can range from simple physical-layout libraries with essentially no links, to packages consisting of layout libraries, simulation models, footprints, and all required interfaces with today's popular EDA environments. Often, the complete library solutions are generated for only one design environment, limiting the flexibility to use alternative tools.

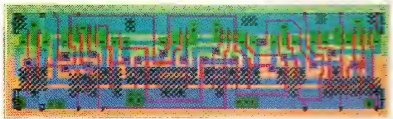
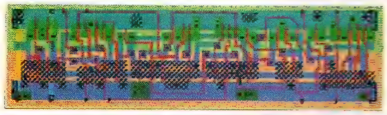
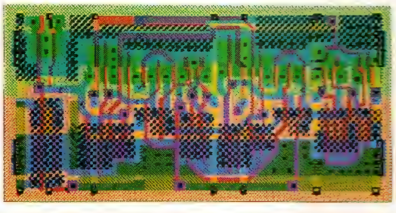
After assessing the designer's needs, it's time to evaluate the product options. An objective evaluation requires a set of guidelines with key parameters that reflect the specific needs and priorities of the designer.

Minimizing chip area is important, and is perhaps the library evaluation criterion that lends itself best to measurement. Designers employ various criteria for area evaluation, including measurement of gates per square mil, transistors per square mil, individual library cell size, and overall chip or block size.

Gates and transistors per square mil appear attractive at the outset because they provide a density measurement that's independent of specific block or chip configuration. However, varying vendor conventions for gate count per function can skew the objectivity of such a measurement *(Table 3)*. The transistor measurement can also be skewed, because transistor count per function can vary widely. For example, increased drive strength can be achieved by adding minimum-size transistors in parallel, or by enlarging one transistor. The latter case will provide a smaller overall block area. However, the former case, though inferior from an area standpoint, will provide a more attractive ratio of transistors per square mil.

In the absence of any standards to regulate methods for gate and tran-

TABLE 2: LIBRARY-ELEMENT VARIATIONS

	Gate count	Transistor count	Relative cell area	Relative routed-block area	Relative delay (cell)	Relative drive strength (cell)
 Density-driven architecture, 1X drive*	11	42	1	1	1	1
 Density-driven architecture, 2X drive*	12	46	1.13	1.03	1.10	2
 Performance-driven architecture, 1X drive*	11	42	1.21	1.15	<0.74	1.6

*JK flip-flop with set and clear functions

TABLE 3: LIBRARY-VENDOR VARIATIONS

Function	Vendor A gate count	Vendor B gate count	Vendor C gate count	Vendor D gate count
2-input AND, 1X drive	2	2	1.5	2
D flip-flop, set and clear, 1X drive	9	9	10.25	9
2-1 noninverting multiplexer, 1X drive	3	2	3.5	2
2-2 OR-AND-invert, 1X drive	3	2	2	2
2 XOR, 1X drive	4	3	3	2.5

sistor counts, the most objective assessment of area consumption is to compare overall block or chip size for a given function. A standardized function or block for this purpose would provide an unbiased and faster benchmarking process. Some low-complexity benchmarking circuits have been proposed as standards by the FPGA industry and others.

Without a standard circuit, designers must formulate their own benchmark circuit. Minimally, such a circuit should contain as much functionality as the designer might need for current and future projects, such as routed blocks of cells, memory components, and other specialized functions. An assessment based on a limited functional library set will lead to a skewed representation of the library capability, and may result in a commitment to a library solution that doesn't meet overall chip-design objectives.

Designers should not overlook performance, power, and drive capabilities in their benchmarking efforts. The requirements for these parameters must be specified, as they can have a great bearing on the area consumed. If they're overlooked, a benchmark may reflect a very dense implementation, but may lack the critical drive or performance to meet system requirements.

Ease-of-use is less quantifiable than area and performance criteria, but often very critical to meeting designers' needs for design productivity and differentiation. One key aspect of ease-of-use is the link between the library solution and a design environment. A complete library solution must provide links to simulation, synthesis, floorplanning, and place-and-route tools. If it does, then it must be determined whether the designer is constrained to work within a specific design environment, or if tools from multiple vendors are supported. Many designers may also find it useful to modify elements or add their own elements to the library. To address this need, the library must interface with physical-design and model-generation tools.

The library's breadth is another critical consideration. Evaluating features such as the number and type of standard cells or gate-array macros, and the availability and flexibility of generators to create optimized blocks for memory, ALU, and datapath functions, can provide valuable insight into the power of a library solution.

The avaiability of a library for the designer's process or foundry of choice should not be overlooked. Designers may want an alternative foundry source. Libraries offered by ASIC vendors and some library providers often target one foundry, and usually aren't rapidly retargetable to different processes.

Today's library-generation techniques make it possible for a designer to specify a process or foundry of choice. Due to the varying techniques used to generate the libraries, designers must consider not only the turnaround time associated with these customized solutions, but also its breadth and flexibility.

Until the nascent commercial-library market matures, perhaps the most critical qualitative criterion in a library evaluation is library-vendor credibility. The level of experience at which library solutions are provided to multiple foundries, the credibility and success of the vendor's library customers, and the vendor's understanding of the needs of IC designers will help gauge the capabilities of a given approach. An assessment of how long a vendor has offered library solutions, to what caliber of customer they provide solutions, and to what extent the vendor is known for providing effective solutions will help give valuable insight into the credibility of the approach.

In the absence of true standards for library evaluation, the individual evaluator is left to define the criteria and to gain an understanding of the trade-offs between different library products. Clearly, the tangible attributes of library products such as area consumption, performance, flexibility, and electronic-design-tool interfaces are critical to the objective evaluation of library solutions, as are less tangible factors like vendor credibility. Until standards are defined, designers are advised to consider the following guidelines in evaluating a library capability:

- Define a benchmark circuit that evaluates chip-level capabilities (include enough functional breadth to evaluate placed-and-routed blocks, memory, ALU, datapath, and so on).
- Define measurement criteria to assess chip area as well as performance and/or drive requirements.
- Discrepancies in definition and architecture make gate or transistor density measurements unreliable—evaluate the overall area of the desired function.
- Determine whether the library offers all links, or the ability to generate links, to the desired EDA tools.
- If modification or addition to the libraries is required, understand the methodology and ease of such modification.
- If process migration is required, determine the time needed to generate the functional library breadth and EDA interfaces.
- Assess the vendor's credibility: How long have they provided library solutions, to what caliber of customer, and how successful are their customers.☐

Harriet Harvey-Horn is the product marketing manager for libraries and process technologies at Compass Design Automation, 1865 Lundy Ave., San Jose, CA 95131; (408) 433-4880. Data research for this article was done by Anil Aggarwal at Compass Design Automation.

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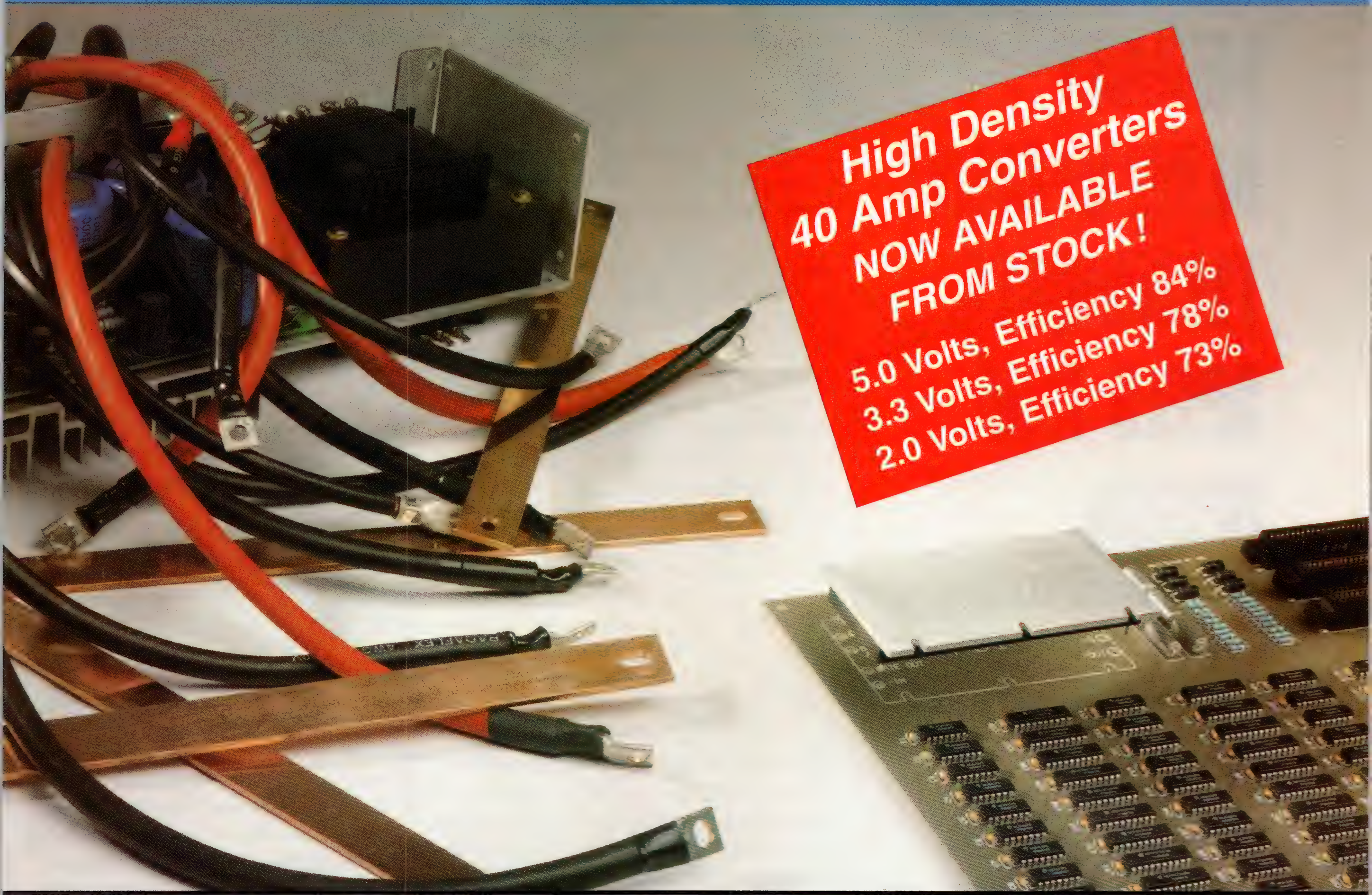
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LIBRARY DEVELOPMENT TECHNIQUES SPEED CHIP DESIGN

RECONFIGURABLE AND PROCESS-PORTABLE LAYOUT SMOOTHS AN IC'S PATH TO SILICON.

BY PHILLIP BRIDE
Mentor Graphics Corp.

Chip design has reached new heights in terms of complexity and speed. Case in point: A North American company had a team of eight engineers design over one million transistors on several chips in less than a year. With the increasing amount of information needed to achieve these complexity levels, design environments must manage and automatically generate scalable chip information.

Advanced library-development techniques can help protect design investment against process, design, and timing changes. Such techniques include:

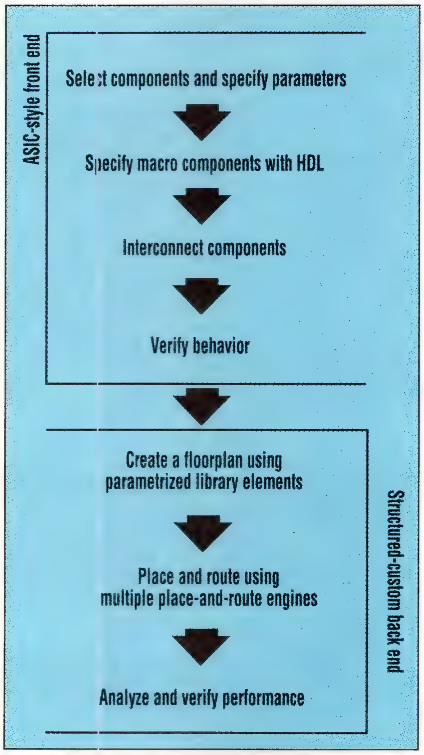
- Process portability combined with module generation, which enables library developers to keep up with their technology group's constant design rule and process changes.
- Graphics generators that let developers quickly create reusable and reconfigurable cells, memories, and datapath elements to meet customer design requirements.
- Automatic characterization of cells that give library developers accurate timing data on the cells and modules, which expedites library-development time.

The need for design re-use is blurring the distinction between traditional custom-IC design and ASIC design, resulting in a convergence into what some are calling full-custom ASIC. Custom-IC designers, who in the past could focus on density and performance at the cost of man-months, now find that they can't afford to stretch out design cycles. On the other hand, ASIC designers find their projects becoming denser, and now require what were once only custom-IC techniques—floorplanning and interconnect timing delays derived from layout.

In the simplest automated design flow, designers begin with a specification, move to a logic or structural stage, and then go to a layout or physical stage *(Fig. 1)*. As the design moves through the flow, it must be translated from the behavioral to the structural level, and then to the physical design. Designers use EDA tools to do the job, and each tool requires a library.

The importance libraries hold in IC designs can't be overemphasized, because they control a design's effectiveness when it gets built in silicon. However, library developers at custom-IC houses and ASIC vendors must deal with a complex development and management problem. For each library element listed in their product guides, they must support up to five other aspects or dimensions for the element. These six dimensions—cell type, cell version, model views, tool environments, processes, and technologies—define the library offering *(Fig. 2)*.

At one time, libraries consisted exclusively of gate- or transistor-level elements, but developers are increasingly offering such modules as RAMs, ROMs, and multipliers. They may even have cores or megacells. Coupling these levels of libraries (cell, module, and core) with the six library dimensions creates an extremely complex library-development problem.


ASIC-style front end
Select components and specify parameters
Specify macro components with HDL
Interconnect components
Verify behavior
Create a floorplan using parametrized library elements
Place and route using multiple place-and-route engines
Analyze and verify performance
Structured-custom back end

1 With the help of automated library-development techniques, traditional design flows will begin to converge into a methodology known as full-custom ASIC design. Because each tool in the flow needs a library, library development is a critical link when translating from the behavioral to the structural level, and then to physical design.

Process portability or technology independence puts importance on layout because it has the most impact on a design. To make a layout cell technology independent, the cell must be implementable into a two- or three-layer metal CMOS or biCMOS process. This is difficult today because each cell has to be laid out in a particular technology. However, each cell can be made process portable. And by focusing on scalable cell design, library developers can accommodate process shrinkage from 0.8 to 0.6 μm or accommodate design-rule changes.

Cell-layout generators written in a language that can access a technology file gives the library developer a means to make the cell process portable. The technology files hold design-rule information specific to the manufacturing process being used and the primitive objects available within the technology. The technology file can then be modified with the

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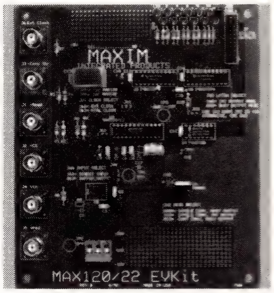

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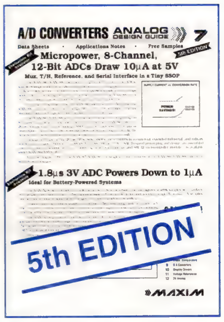
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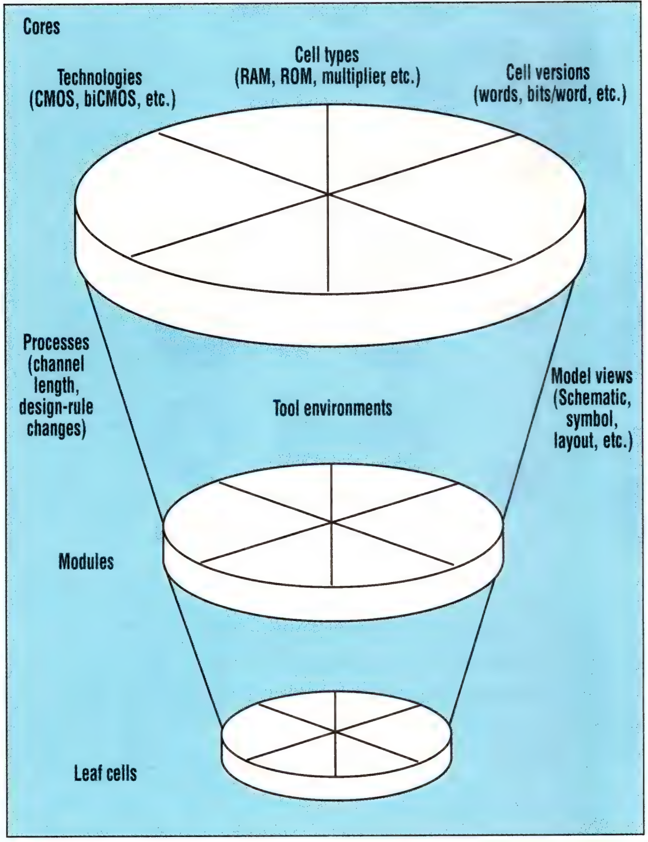
IC LIBRARY DEVELOPMENT


Cores
Technologies (CMOS, biCMOS, etc.)
Cell types (RAM, ROM, multiplier, etc.)
Cell versions (words, bits/word, etc.)
Processes (channel length, design-rule changes)
Tool environments
Model views (Schematic, symbol, layout, etc.)
Modules
Leaf cells

2 **This illustration shows the complex problems associated with library development at the leaf-cell, module, and core levels. Each level of library development is complicated by the need to define six dimensions for each element: cell type, cell version, model views, tool environments, processes, and technologies. The result is an enormous array of elements that need to be recreated when migrating a design to another process.**

new design rules or process data, and the cell generators rerun to port them to the new process.

Modifying a technology file assumes the cell generator was built to handle process and design-rule changes. Incremental compaction plays a crucial role in process portability. It lets library developers build process-portable generators that position objects as close as possible and aligns the edges of diffusion. This makes design-rule changes possible and helps automate the task so that library developers need not wait for the technology to be completed before starting the library effort. They can build their libraries concurrently with the technology development, shortening the time it takes to get their library to the customers.

Module and cell generators allow each library element to offer a list with parameter choices, such as drive strength, number of inputs for cells, bits-per-word, and word depth. Then, after selection, layout, schematic, symbol, and timing are created automatically.

For example, take a NAND-gate cell generator that's written for 0.8-μm three-layer-metal CMOS. A cell generator might have the number of inputs and drive strengths parametrized. That way, library developers could create numerous versions of the NAND gate very quickly, including layout, timing, symbols, and functional model for each of the gate configurations.

Module generators, which are built for reconfigurability, make considerable use of RAMs, ROMs, PLAs, multipliers, adders, ALUs, and various regular structures. For example, a synchronous, static, dual-port RAM generator may offer multiplexing options for aspect ratios, and may have output options such as tri-state or bus keeper, number of words, and bits per word.

Traditionally, module-generation design meant writing code. However, the graphical module-generator capture systems employed today put users back into a design domain much more suitable for memory or datapath creation. This new capability takes the form of a floorplan with bounding boxes delineating the design's various subsections or leaf cells. With these techniques, users can build sophisticated reconfigurable designs in about the same amount of time it takes to build a fixed-module configuration.

The real advantage is realized when new configurations are needed. The generator creates a new layout, timing models, symbols, and a functional model in a fraction of the time it would take a developer to redesign the module, even if starting from an existing one. For example, using module generation, library developers could create, characterize, and verify all of the models for a 4-kword-by-32-bit RAM in less than two days. Completing this task manually would take weeks.

ASIC vendors often wait until the technology is complete before starting on the cell layout for library elements. But with cell generators, ASIC vendors can start layout during technology development because they have a vehicle to respond to design-rule changes on the fly.

Generally, it's timing that kills designs. Critical paths preclude the design from operating at speed. An erroneous estimation of the cell delays or an inaccurate net-delay calculation points to the wrong critical path. To help chip designers avoid these problems, library developers must provide accurate timing for the models at the cell and module level.

The most common practice involves laying out the cells, extracting or estimating capacitance/resistance values, and building a simulation model of the cell. Library developers simulate the cell's structural model at the analog level, often with a Spice simulator. This simulation enables them to gauge input delays, transport delays, skew and slew information, output delays, and other information as required.

Design teams use many types of timing equations to estimate the timing of their cells: 3-to-N-term equations, piecewise linear models, and others. Whatever model the designer uses, it's important to build an automated flow to capture the timing directly from layout. To make the data useful, library developers must back-annotate into the simulation model. They must also place the information into data-sheet format for use in behavioral simulation models and synthesis rules, or for data-sheet use.☐

Phillip Bride works in product marketing in the IC division of Mentor Graphics Corp., 8005 S.W. Boeckman Rd., Wilsonville, OR 97070; (503) 685-7000.

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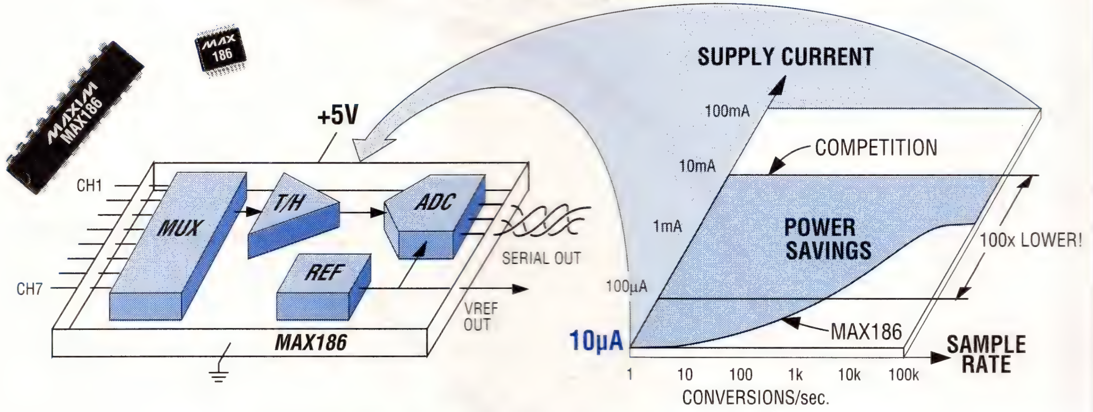

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MAX191	Parallel	1	INT	100ksps	50µA	24	$9.60	MAX191EVSYS

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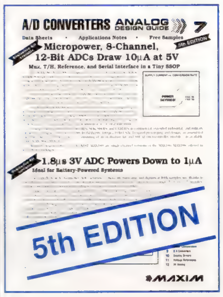
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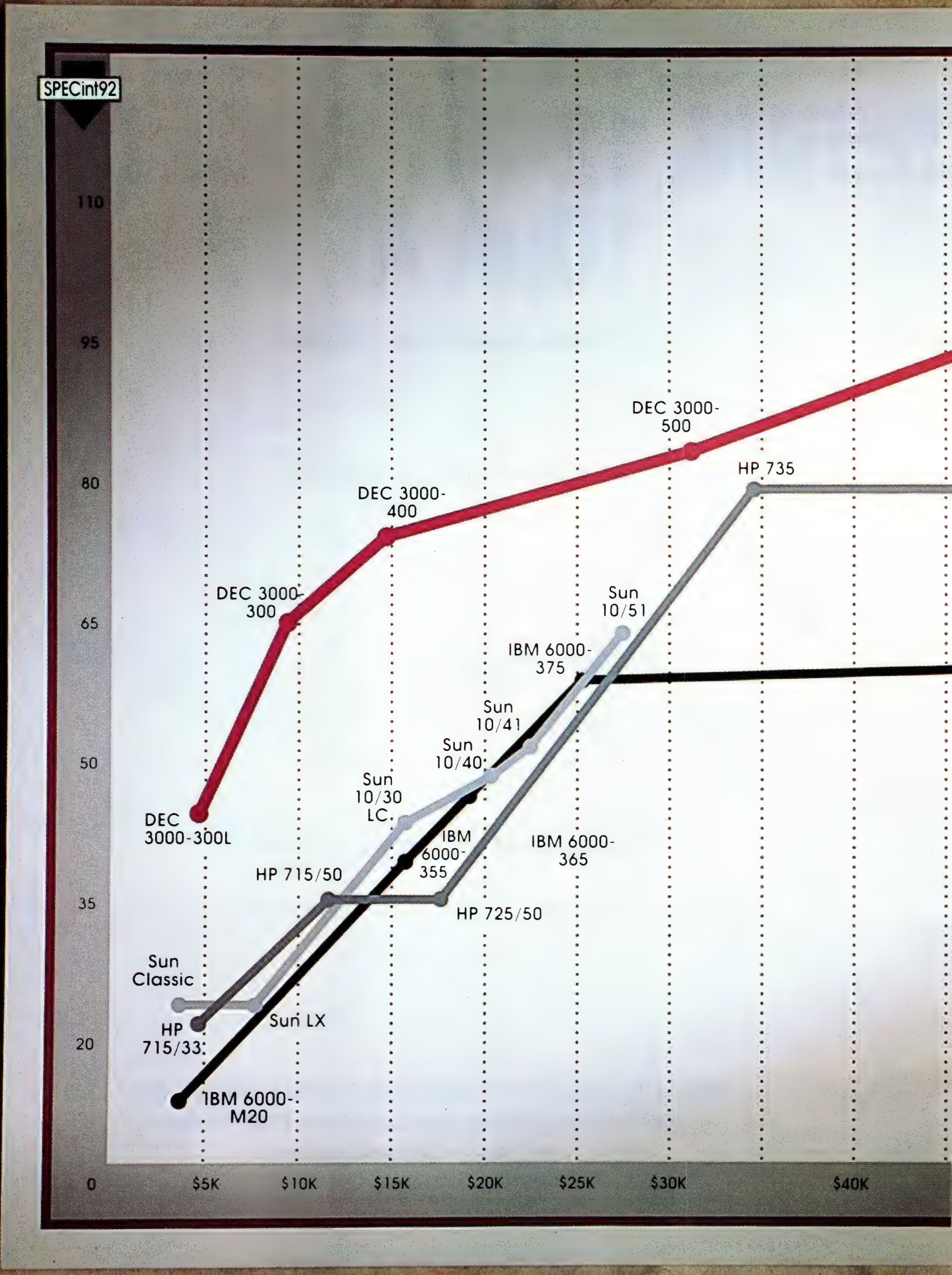

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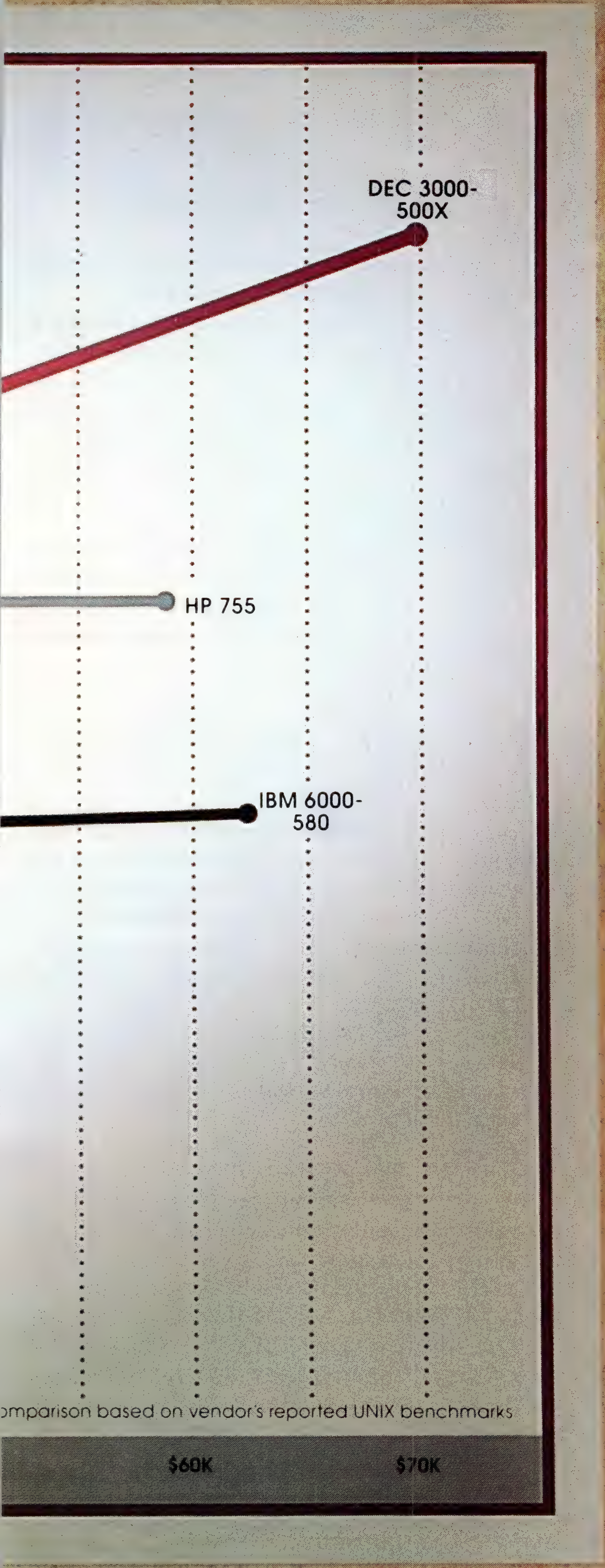

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PROPER DATA MANAGEMENT STRENGTHENS DESIGN QUALITY

ACCURATE INFORMATION IS ESSENTIAL FOR COMPLEX SYSTEM DESIGN.

BY JOSEPH CAREY, NEAL HARRISON, AND THOMAS PENNINO
AT&T Bell Laboratories

Computer-aided-design (CAD) software is essentially worthless without the underlying component information it requires. One of the most difficult questions facing today's designers of complex electronic systems is how to get complete and correct component data during the design cycle and through the manufacturing process.

With 80% of the cost of electronic products attributable to electrical components, it makes good sense to focus on cost-effective component selection. Throughout the product-realization process (PRP), daily component decisions are made that directly affect the cost, reliability, and quality of products being designed or manufactured.

A comprehensive component-data-management system ensures that the most cost-effective electrical components are used, and that complete and correct information about those components is available throughout the product cycle. Though the concept can be simply stated, effective component-information management is a complex and ongoing task. Component-management systems yield significant benefits in time-to-market, cost, and quality of an end product. They also provide a foundation for the planned introduction of new technology and computer aids.

The component-management task is simplified by treating it as two subtasks—component-information management and component-library management. Component-information management makes sure that the most cost-effective components are used, and component-library management assures the availability of complete and correct information to drive the computer-aided-design tools throughout the product design cycle. Although this separation helps explain the tasks, these two areas are actually highly integrated both operationally and at the data model.

Componenet-information management (CIM) is the efficient and timely management of component information to ensure that reliable, high-quality, competitively priced components are available and used throughout the life-cycle of the products being built. The implementation of CIM must be pervasive throughout the product-realization process (from architecture definition through the design and manufacturing cycles) *(Fig. 1)*. In fact, it's actually an ongoing task throughout the life of the product.

A complete CIM system may consist of a preferred-parts list, stocklist management, component selection, and administration and tracking. These functions are interrelated and need to be supported by one automated component-management system.

The preferred-parts list is the list of components approved for use within a company or on a specific project. Components on this list are determined by the company's component engineers to be cost-effective parts that conform to component-technology, packaging, and assembly strategies. In addition, the parts have survived component- and supplier-qualification processes. The following information is attached to each component on this list:

- Complete functional and electrical characterization of the part.
- Equivalent components that have also been approved for use. This information enables the factory to make cost trade-offs over time and permits part substitution by the factory on short notice. This mechanism also manages global manufacturing requirements where agreements may require the use of local devices. It essentially allows a domestic factory to use one part while a foreign factory employs a pre-approved equivalent.
- Component keys that name the part so that people and software systems can reference it throughout the product-realization process. Failure to manage component keys results in "alignment" problems across systems and databases throughout the PRP, and will cause serious delays in the interval because of potential misinterpretation in factory manufacturing-resource-planning (MRP) operation.
- Notes carrying information that's not formally part of the data model.
- Ordering and packaging information.

The preferred-parts list represents parts pre-approved by the component engineer. The approval process generally involves the component and product engineers, and corporate supply-line management organization. It's the circuit designer, however, that actually selects the components to be used on a particular design from among the parts already approved for use.

Stocklist management is an integral part of the component-management system. In fact, it's the primary vehicle for sharing component-usage information on a product-by-product basis between design and manufacturing. Multiple versions of the stocklist are maintained for products in the development, manufacturing, engineering, and factory-production environments.

The stocklist flows electronically between design and factory, thereby

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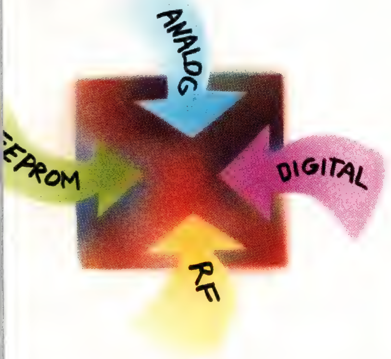

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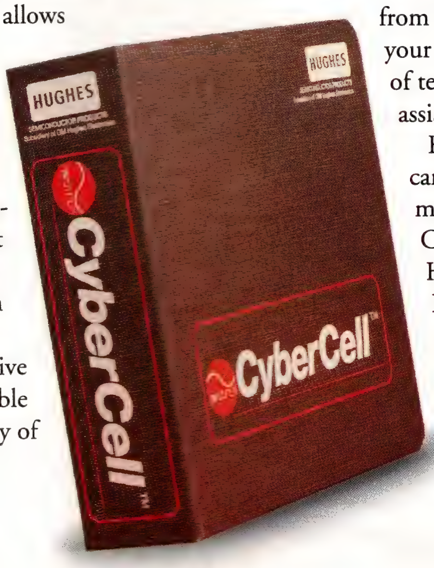

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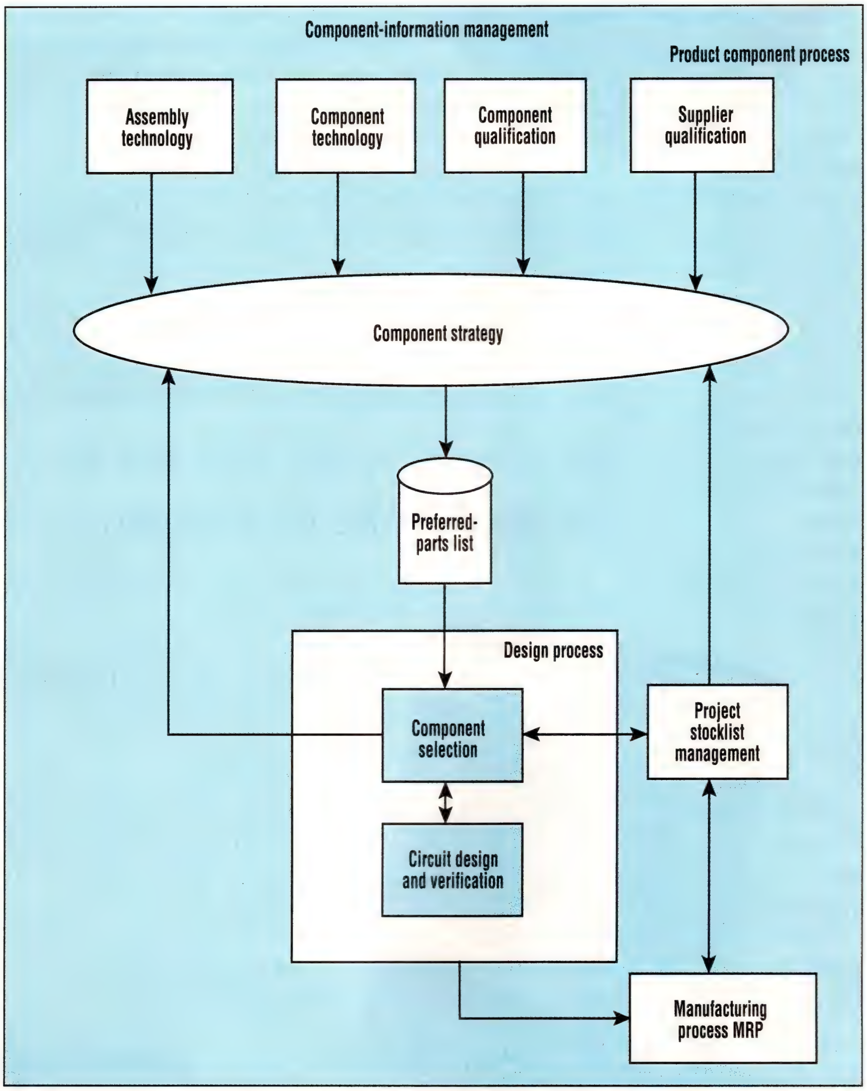
reducing errors resulting from reentry, and encouraging information sharing. The stocklist is initiated very early in the design process. Initial versions of the stocklist, along with "confidence" levels for each component that indicate the degree of certainty a component will be used in manufacturing the end product, are shared with the factory-component engineer.

Query functions that operate throughout the component-management system provide access to reliable and timely information to support cost-effective component decisions. They support interrogation of component, product, process, and administrative data. This includes interrogation of approval and availability status and the electrical and functional attributes within the preferred-parts list.

The query function also provides interrogation of stocklists of other products. Essentially, this gives the engineer insight on component usage within the company. These functions are used daily by designers, factory-component and product engineers, and managers. Ultimately, the query functions help to reduce product cost and also to ensure product quality.

The system should track requests for new component approval, and the subsequent acceptance or rejection of the part. To monitor and control component usage across the product and company, audits can compare current stocklists with the current preferred-parts list and flag the use of unapproved parts. The circuit designer and the component engineer use this mechanism to ensure conformance to the company's component strategies. Conformance also occurs by integrating control mechanisms in the stocklist and factory systems to ensure the same preferred-parts list is employed throughout the design and manufacturing processes.



1 A complete component-information-management system consists of a preferred-parts list, stocklist management, component selection, administration, and tracking.

Component management is an ongoing task that continues through the life of the product; it doesn't end with product manufacture. Electronic products are constructed using a variety of ICs, and the life cycle (defined as the period of time that these components are available from multiple suppliers at competitive prices) of many of these components is significantly shorter than the lifetime of the end product. Component life-cycle information is tracked on an ongoing basis. As components approach latter stages (decline and phase-out), the component-management system identifies end products in which they're used. Decisions are then made as to whether product redesign is necessary.

COMPONENT CHOICES

Component choices help define manufacturing-technology and component-life-cycle projections and are applied in the formulation of preferred-parts lists. The component-selection mechanisms utilized by the circuit designer are populated with preferred-parts lists, and evolving stocklists for each design are audited against the same preferred-parts list. CAD component libraries contain preferred parts, as do downstream factory-MRP and bill-of-materials systems.

CAD software permeates the entire design process, from schematic capture, simulation, and timing analysis, through layout and thermal analysis. The required component information varies with the software's function, and it must be provided in the file format expected by the design-automation software. That required information is the software's component library.

Adding a new component necessitates different data in all supporting CAD component libraries, such as the schematic-symbol, layout, simu-

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	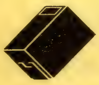	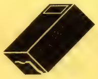	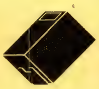		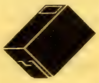		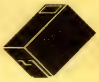	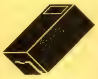	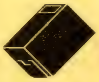	
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330 µF	220 µF	100 µF	100 µF	47 µF	68 µF	33 µF	33 µF	22 µF	22 µF	10 µF
100 mΩ ESR	100 mΩ ESR	100 mΩ ESR	100 mΩ ESR	150 mΩ ESR	150 mΩ ESR	200 mΩ ESR	200 mΩ ESR	300 mΩ ESR	300 mΩ ESR	300 mΩ ESR
D case size = EIA 7343 E case size = EIA 7343H										

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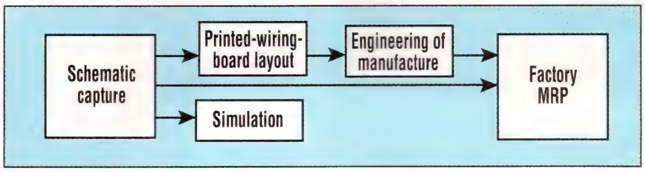
COMPONENT-DATA MANAGEMENT

lation, timing, and thermal libraries. This assumes the same CAD tools are used throughout the company or project. If multiple schematic-capture and layout tools are used, then entries are needed in the separate component libraries associated with each tool.

CAD systems don't generally share their libraries. Therefore, each system requires a custom library. This isn't a complete duplication of effort because each system adds unique component-data requirements, but the separate engineering of these libraries impedes the electronic flow of design information. Problems with aligning libraries include both the inconsistent representation of key data fields and the lack of coverage (components represented in one library, but not in others).

Other alignment problems occur between component libraries and the preferred parts and factory bill of materials in the corresponding MRP system. The design delays caused by unaligned component libraries can be significant, and generally occur at the major handoffs in the product-realization process *(Fig. 2)*.



2 **Alignment problems may occur between component libraries and the preferred parts and the factory bill of materials in the corresponding MRP system. Design delays caused by alignment mishaps can be significant, and generally occur at the major handoffs in the product-realization process.**

ENSURING ALIGNMENT

To ease the alignment problem, one component library should serve the entire product design process. All entry into the library is controlled and verification functions must be included to audit component definitions for completeness and consistency. To ensure alignment with component-management and factory-MRP operations, a well-defined process should be established to ensure that all components in the preferred-parts list are represented in both the library and the manufacturing-resource-planning system. Library-system and MRP-system entries may be triggered electronically from the component-management operations, thus guaranteeing coverage and key alignment.

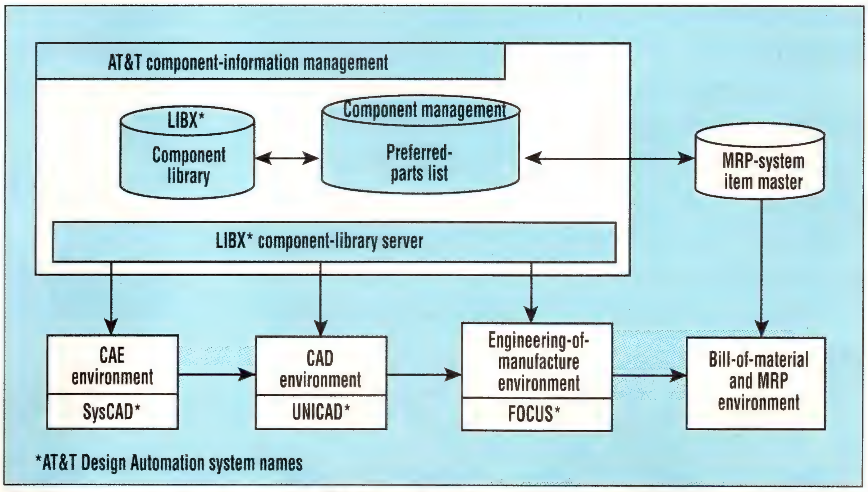
Considerable investments are made in component libraries, therefore ensuring correctness and completeness of the data is essential. Unfortunately, the value of these libraries diminishes greatly when migrating to new tools. To maximize long-term value of CAD component libraries, component-library systems must be CAD-tool independent. The internal data model and data-storage format need not be known by the design-automation-system application software.

CAD system access to the data is defined at the software-development level. Consequently, each application defines the data it requires and the format in which it would like to receive that data. This library-server architecture enables both the library system and the applications to evolve and be deployed independent of one another *(Fig. 3)*. Applications can change the content and format of the data they desire without invalidating the existing libraries. This same architecture enables many computer-aided-design applications and factory systems to utilize the same library.

The component library is established as the single source of certified data. All preferred parts have complete entries in this library. Unapproved parts may also be resident in the library, which enables preliminary (or prototype) use, pending approval. If design activity is spread out over a number of locations (nationally and internationally), it will be necessary to maintain copies of the component library at remote locations. The system will also include distribution software to incrementally update new and changed data to the remote sites.

The concept of a CAD-system-independent library enables a company to carry library data through the evolution of computing platforms and evolving CAD software. This same concept can be applied when reusing library data with multiple-vendor computer aids. In each case, the breadth and depth of the data model makes it possible to transform component-library entries to the format required by a vendor system. A component library server is utilized to access the library definition so that the library and the computer-aided-design software can evolve independently *(Fig. 4)*.

A broad data model is necessary to serve application software through-


AT&T component-information management
LIBX*
Component library
Component management
Preferred-parts list
MRP-system item master
LIBX* component-library server
CAE environment
SysCAD*
CAD environment
UNICAD*
Engineering-of-manufacture environment
FOCUS*
Bill-of-material and MRP environment
*AT&T Design Automation system names

3 **To maximize the long-term value of CAD component libraries, component-library systems need to be tool-independent. The internal data model and data-storage format needn't be known by the application software because CAD system access to the data is defined at the software-development level. As a result, each application defines the data it requires and the format in which it would like to receive that data. This library-server architecture enables both the library system and the applications to evolve and be deployed independent of each other.**

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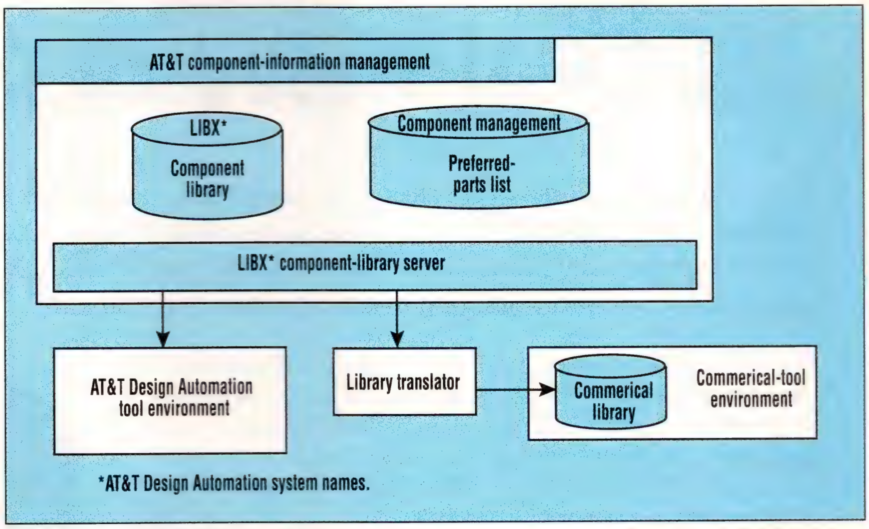
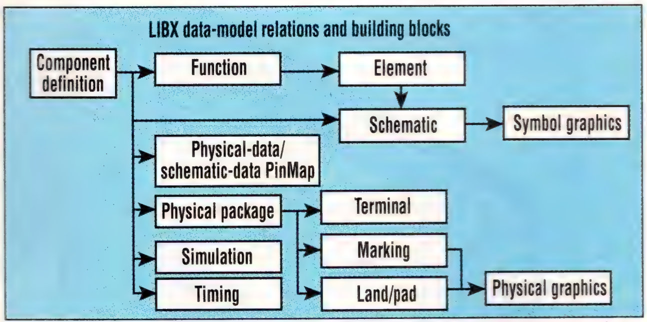

AT&T component-information management
LIBX*
Component library
Component management
Preferred-parts list
LIBX* component-library server
AT&T Design Automation tool environment
Library translator
Commerical library
Commerical-tool environment
*AT&T Design Automation system names.

4 The concept of a CAD-system-independent library enables a company to carry library data through the evolution of computing platforms and evolving CAD software. This same concept can be utilized in reusing library data with multiple-vendor computer aids.

out the design and manufacturing process *(Fig. 5)*. The applications include schematic capture, simulation and timing analysis, placement and routing, thermal analysis, engineering of manufacture, assembly drawings, and complete physical-package characterization supporting numerical control outputs for component insertion and placement.



5 A broad data model is necessary to serve application software throughout the design and manufacturing process. The applications include schematic capture, simulation and timing analysis, placement and routing, thermal analysis, engineering of manufacture, assembly drawings, and physical-package characterization supporting numerical control outputs for component insertion and placement.

The physical implementation of the library data model can share a significant amount of data. The simplest example involves a 16-pin plastic DIP with pins on 100-mil centers. Hundreds of components in the library may come in this physical package, but the package need only be stored once. Similar data sharing occurs in the schematic symbol area where gate-level symbols are referenced to create packages of gates. A generic design code represented by four NAND gates may appear only once in the library, but is referenced by many component definitions. Mapping of schematic symbols to physical pins enables components to share symbol graphics even when pinouts on the physical device are different. This data sharing is efficient in storage space, and makes library entry very straightforward.

The data model should also support the bare-board topology definition, and hardware parts like heat sinks and latches. The engineer associates hardware parts with the board definitions, so that when a board is loaded into a design, it's complete.☐

Joseph Carey is CAD sales and customer service manager, Neal Harrison works as a technical manager in computer information systems development, and Thomas Pennino is the department head of the circuit pack CAD department at AT&T Bell Laboratories, Crawfords Corner Rd., Holmdel, NJ 07733; (908) 949-3000.

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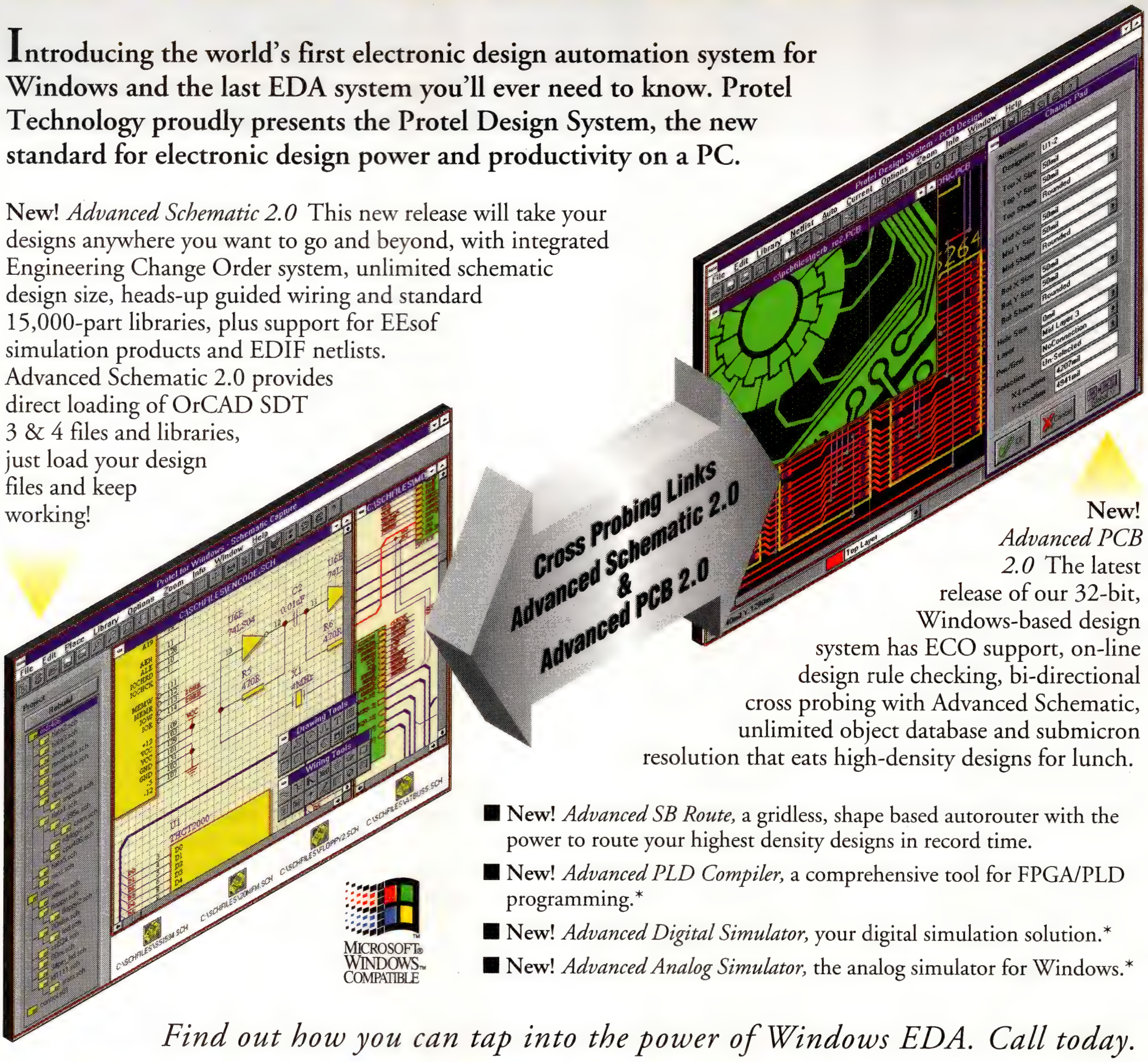

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CIRCLE 165 FOR U.S. RESPONSE   CIRCLE 166 FOR RESPONSE OUTSIDE THE U.S.

ELECTRONIC DESIGN QUICKLOOK

EDITED BY SHERRIE VAN TYLE

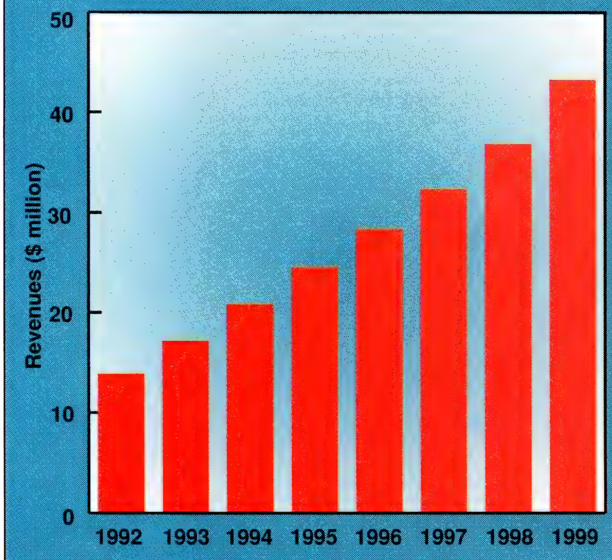
MARKET FACTS

With personal communication services (PCS) growing out of cellular, the U. S. mobile communication services market will more than triple by decade's end, going from $13.9 billion last year to more than $43 billion by 1999, according to a study by Frost & Sullivan Market Intelligence, *Mobile Communication Service Markets: Enhanced Offerings Expand User Base.*

The Mountain View, Calif., market researchers predict that cellular phone growth will slow with the beginning of saturation in prime end-user groups, the increasing introduction of PCS as well as specialized mobile radio in more metropolitan areas, and the trend for subscribers to spend less time on their mobile phones. Meanwhile cellular growth rates will hover at around 30% until PCS chips away at that sector while paging's growth rate should stay in the teens. By the end of the decade, mobile satellite services will deliver various data and video applications.

Personal digital assistants (PDAs), relying on wireless technologies, will eventually dial emergency numbers, set up appointments, and read on-board vehicle diagnostics. A PDA could reserve a technical journal in a library, book a reservation, order supplies, and pay bills. Frost & Sullivan Market Intelligence also predicts that landline and mobile phones will gradually merge with PCS handsets and data devices working on a seamless telephone network. The subscriber base, once dominated by executive and sales and service workers, will be joined by users working in health and security areas, delivery persons, and personal users interested in security.

MARKET FOR U.S. MOBILE COMMUNICATIONS SERVICES IS ON THE MOVE



Compound annual growth rate (1992-1999): 17.7%
Source: Frost & Sullivan Market Intelligence

EYE ON ISO 9000

Micro Networks has been registered under ISO 9001. The company, a division of Unitrode Corp., supplies high performance components for data conversion—analog-to-digital converters, digital-to-analog converters, amplifiers, data-acquisition systems, custom hybrids, and precision oscillators; it is located at 324 Clark St., Worcester, MA 01606-1293; (508) 852-5400; fax (508) 853-8296. CIRCLE 480

Sequent Computer Systems has received ISO 9001 certification for the company's Unix-based computer systems. Sequent's Beaverton, Ore., facility has gained certification for contracted computer maintenance services supplied by the company's service organizations in North America and the U. K. The company is located at 15450 SW Koll Pkwy., Beaverton, OR 97006; (503) 626-5700. CIRCLE 481

NKK Switches has received ISO 9001 certification. The Scottsdale, Ariz., company has toggle, rocker, pushbutton, slide, keylock, illuminated, rotary, and custom switches. The company is located at 7850 E. Gelding Drive, Scottsdale, AZ 85260; (602) 991-0942; fax (602) 998-1435. CIRCLE 482

AT&T Microelectronics' Henrico County plant, near Richmond, Va., which manufactures the company's multilayer printed-circuit boards for telecommunication products, has received ISO 9002 certification. For more information, contact AT&T Microelectronics, Dept. 500404200, 555 Union Blvd., Allentown, PA 18103. CIRCLE 483

Crydom, a manufacturer of solid-state relays, received certification for meeting ISO 9002 standards. The company is located at 6015 Obispo Ave., Long Beach, CA 90805; (800) 827-9366; fax (310) 865-3318. CIRCLE 484

M-tron Industries, a maker of quartz crystals and hybrid oscillators, has received certification to ISO 9001, the first such U. S. manufacturer to do so, the company says. M-tron Industries can be reached at P. O. Box 630, Yankton, SD 57078; (800) 762-8800; (605) 665-9321; fax (605) 665-1709. CIRCLE 485

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	28 PLCC	44 PLCC	68 PLCC	84 PLCC	100 PQFP	144 PQFP	160 PQFP
PLCC	20 SOIC	28 PLCC	44 PLCC	68 PLCC	84 PLCC	100 PQFP	144 PQFP
PQFP	16 SOIC	20 SOIC	28 PLCC	44 PLCC	68 PLCC	84 PLCC	100 PQFP
SOIC					44 PLCC	68 PLCC	84 PLCC
						44 PLCC	68 PLCC

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QUICKLOOK

OFFERS YOU CAN'T REFUSE

Analog Devices' ADSpice library disk, consisting of 352 models—34 of them new—includes the industry's first macromodels for a CMOS analog switch, variable-gain amplifier, and video difference amplifier. Besides these innovative models, ADSpice features many of the company's op amps, instrumentation amplifiers, analog multipliers, voltage references, and matched transistor pairs. New models of the company's family of switches include parameters such as turn-on time, charge injection, feedthrough, ON resistance modulation, and crosstalk. These models reflect the use of complementary n-MOS and PMOS transistors to enhance device characteristics.

To obtain the free 5.25-in. IBM PC-compatible floppy disk, contact Analog Devices Literature Center, 70 Shawmut Rd., Canton, MA 0201; (617) 821-4273. CIRCLE 488

MINC's PC-based PLDesigner-XL Prodigy system is free of charge to users who purchase a year of support services from the company. PLDesigner-XL Prodigy supplies an advanced environment for the design of all types of programmable logic technologies, including FPGAs, complex PLDs, and basic PLDs. To qualify, users must submit their purchase orders to MINC with proof-of-purchase for their existing non-MINC software. With the purchase of MINC support services ($750) users will receive the PC-based PLDesigner-SL Prodigy software (ordinarily $2995), a disk containing a design translator utility compatible with Data I/O's ABEL 4 language, including software updates and unlimited access to MINC's customer support staff. The offer is good in the U. S. through Oct. 31, 1993.

For further information, contact MINC, 6755 Earl Drive, Colorado Springs, CO 80918; (800) 755-3742. CIRCLE 489

Knightline is a new technical newsletter with information on Knights Technology's products, technology developments, and software applications in three areas of semiconductor manufacturing software: CAD navigation, yield enhancement, and test programming.

Published three times a year, the Knightline newsletter is available free of charge by writing on company letterhead to Knights Technology Inc., 155 North Wolfe Rd., Sunnyvale, CA 94086; fax 739-4438. CIRCLE 490

DID YOU KNOW?

. . . that ownership of fax equipment for home offices jumped dramatically last year with 47% of home offices and 89% of work-at-home owners reporting that they had owned their fax units for less than a year. Devices were purchased because workers thought they were losing business without one (51%) while 41% of work-at-home households bought a device to communicate with the office. Lower fax prices prompted less than 5% of home office sales and less than 18% of work-at-home households to purchase the devices.

A survey of 150 households by BIS Strategic Decisions, (617) 982-9500.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 443, 100 Prickly Pear Rd., Verdi, NV 89439; (408) 446-4458; fax (408) 253-6085

As the definition phase nears completion, attention shifts to planning and fully staffing the execution phase. While growing staff from the 20% level to the 100% level might appear to be a major problem, it's often easier to accomplish than staffing the definition phase. Why is it less difficult? The answer lies in the number of available alternatives that can be used to provide execution phase staffing. As such, this column begins to explore methods by which the execution phase can be staffed to the 100% level in a short time.

Available sources of execution phase staff include staff already assigned to the project's definition phase, transfers from other projects, transfers from other internal work groups, experienced hires, college hires, internal contractors, and external contractors. If the execution phase staff is formed by retaining definition phase members and equally utilizing the remaining six sources, each classification would contribute about 12% of the total. As a result, a 24 person cross-functional execution phase team could be formed as illustrated in the table.

Source of staff	No. on 24 person E-phase	% of total
Continue from definition phase	6	25%
Other project transfer	3	12.5%
Other internal transfer	3	12.5%
Experienced new hires	3	12.5%
College new hires	3	12.5%
Internal subcontractors	3	12.5%
External subcontractors	3	12.5%

On the surface, forming a 24-person team from seven sources of talent looks relatively easy. Six people are already in place on the project's definition phase. Six of the remaining 18 come from internal transfers, 6 from new hiring programs, and 6 from two sources of subcontracting. To make it happen, a company needs to understand how to effectively move internal resources from work group to work group and from one project to another; run college and professional recruitment programs; and use contractors effectively. All functions and work groups need to have their staff management practices act together. It's an easy job doing all these things if there is minimal sensitivity to time. However, time-to-market-focused organizations have to learn how to staff fast.

To get an execution phase done quickly, a product development organization has to staff it to capacity quickly. That's the part that takes skill and organizational effectiveness. Yes, even the human resources department gets actively involved in reduced time-to-market product development programs! Companies that know how to do it are time to market winners. They have a significant competitive advantage over those who bungle fully staffing their time sensitive projects!

More information on this topic is contained in New Product Development: Design and Analysis, which can be obtained by calling Time to Market Associates.

QUICK NEWS

The ANSI/IEEE Standard 1596-1992 Scalable Coherent Interface (SCI) specification gives users a one-chip interface that includes transceivers, FIFOs, and protocol logic. This interface supplies computer-bus-like services but delivers higher system performance than a bus supplies. The published standard has executable C routines in an ASCII text file (Unix shell script) on an IBM-format 3.5-in. disk that accompanies the printed specification. The SCI standard (item code SH15255) can be ordered from the IEEE service center at (800) 678-4333 or (908) 562-3800; fax 981-9667. The price is $68, plus $4 handling.

TALES FROM A SKUNK WORKS

My past two columns contrasted differences in management style between the companies that are leading in the 90s, and those that are still trapped in the past. If companies were life forms, the top 10% firms and the bottom 80% might have evolved on different planets.

We studied how Japan Air Lines reacted to disaster. The airline apologized and self-corrected. The company helped the grieving relatives for years. Some of those responsible resigned; some even committed suicide. Trust was restored.

Contrast that to the traditional U. S. combination of micro-management and bureaucracy. Hanford dumped radioactive materials for decades. This broke no rules at the time. Victims in surrounding towns now have the impossible task of "proving" that their specific cancers stemmed from radiation releases long ago. Trust is low, so litigation and gridlock result.

When I use these examples in lectures, the reaction is disbelief. The fact that some Japanese maintenance workers chose suicide because they felt they let the team down generates the most intense reaction.

I stress that the normal "punishment" in progressive team cultures is just the general knowledge that you screwed up. This permits learning and progress. If the existence of the firm or its reputation is not threatened by the error, life goes on smoothly.

In 1968, another Japan Air Lines incident occurred. Captain Kohei Asoh landed a DC-8 jetliner short of the runway at San Francisco. The aircraft made a perfect touchdown in a few feet of water, and the crew evacuated the 96 passengers safely. There were no injuries, and the aircraft suffered only minor damage.

The station manager for San Francisco did a very un-Japanese thing. After thought, but without consultation or consensus and knowingly breaking all the rules, he instructed that no calls from Tokyo were to be accepted. Then he met the unhappy passengers. They were shaken, and their luggage was sitting on the bottom of San Francisco Bay.

The manager offered a sincere apology and told them to buy whatever they chose at JAL expense to replace belongings. This resulted in some lavish purchases, but it was a good investment. There was no litigation, and the station manager went unpunished for his impulsive violation of other's roles. Since the incident was under the purview of the U .S., the National Transportation Safety Board assembled for the traditional multiyear legal finger-pointing exercise to place blame. The first question: "Captain Asoh, in your own words, can you tell us how you managed to land that DC-8 stretch jet 2 1/2 miles out in San Francisco Bay in perfect compass line with the runway?"

The answer, which was never recorded, is a legend in the industry. "How you Americans say? Asoh ---- up!" The hearing was quite brief. After interviews with JAL management and medical exams, Captain Asoh flew the line until his retirement in the late 1980s. I think he would have done well in a skunk works. (This example is from Peter M. Senge's book, *The Fifth Discipline*, which I highly recommend.)

John D. Trudel lectures and provides business development consulting. Trudel is founder and director of The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 690-3300; fax (503) 543-6361; e-mail address: JohnTrudel@aol.com. He is the author of High Tech with Low Risk. *To order, phone (503) 280-8547.*

HOT PC PRODUCTS

Nothing is more frustrating than turning on a PC and watching the system unsuccessfully try to boot up. Typically, a user pulls out a diagnostic program or utility for DOS. The Micro Scope 5.0 utility from Micro 2000 gives troubleshooters more flexibility by avoiding DOS and performing diagnostics by running its own OS.

The software runs on any Intel or Intel-compatible processor and can troubleshoot any PC or PC-compatible. In addition to the software, the utility comes with three loop-back port-test plugs. Assuming the system turns on and tries to read a disk in the A drive, the diagnostic boots on the computer using only 2 kbytes of memory. Memory testing can then be done to verify the rest of the base memory—something not easily done with DOS-based diagnostics.

Once the memory is verified, the rest of the menu-driven utility is loaded. The software breaks down system information into categories such as system configuration, active ROM search, IRQ assignments, partition tables, CMOS display/edit (for systems with CMOS backup RAM), and show POS registers (for PS/2 systems). Disk partitions can be repaired, CMOS files edited, and critical PS/2 setup information can be displayed.

Diagnostics cover system-board, coprocessor, memory (base, cache, extended), floppy disk (up to the 2.88-Mbyte units), fixed-disk, serial port, parallel port, and video testing. Utilities include memory display, floppy editor, fixed disk editor, rebuild masterboot, floppy head cleaner, toggle attributes, and version information. All real-mode memory can be displayed and all areas on floppy and fixed disks can be displayed and edited, including track 0.

The Micro Scope 5.0 software, which sells for $499, comes with 3.5- and 5.25-in. disks, loopback plugs, and 178-page manual. Contact Micro 2000 Inc., 1100 E. Broadway, Glendale, CA 91205; (818) 547-0125.—DAVE BURSKY-

CIRCLE 486

A leather disk holder carries two 3.5-in. disks and a business card; in black or burgundy, the handmade case can be used for software presentations to customers or simply to carry disks from work to home. Cases are $15.95 each, or six for $89, plus shipping. Volume discounts apply on orders of 12 or more. For information, contact Browning & Drum, P. O. Box 468, Brookline Village, MA 02147; (617) 566-4300; fax -4208.

CIRCLE 487

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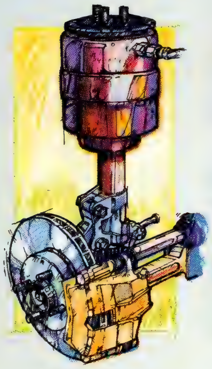

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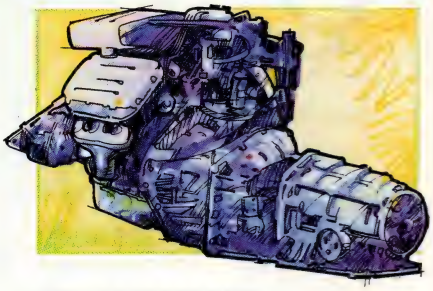

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INSTRUMENTATION

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- H-Bridge Power ICs for HVAC & Gauge Control
- Hall-effect Window Position Sensors
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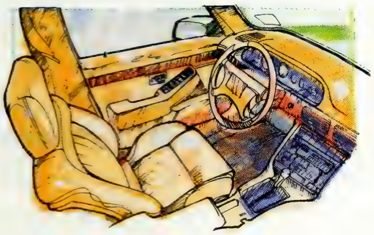

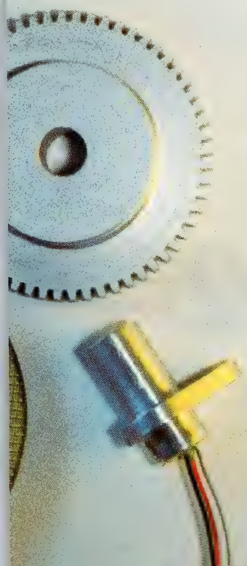

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CIRCLE 167 FOR U.S. RESPONSE CIRCLE 168 FOR RESPONSE OUTSIDE THE U.S.

CIRCLE 521

Measure True RMS Lamp Voltage

JOHN DUNN
181 Marion Ave., Merrick, NY 11566.

When driving incandescent lamps from a display driver such as the Allegro Microsystems UCN5824A, the true rms voltage applied to the lamp filaments may require measurement. That can be a problem, though, because the multiplexed lamps receive unipolar pulses of voltage that are switched during the multiplexing operation per each driver's Output Enable pin. Some so-called true-rms DVMs measure rms values through a dc block. Therefore, obtaining meaningful results for these lamps can be a difficult chore.

However, by setting the display for all eights and obtaining the lamp drive waveform *(see the figure)*, any average-responding dc voltmeter can be used to measure the true rms voltage. The measurement involves some calculations using the following relationship:

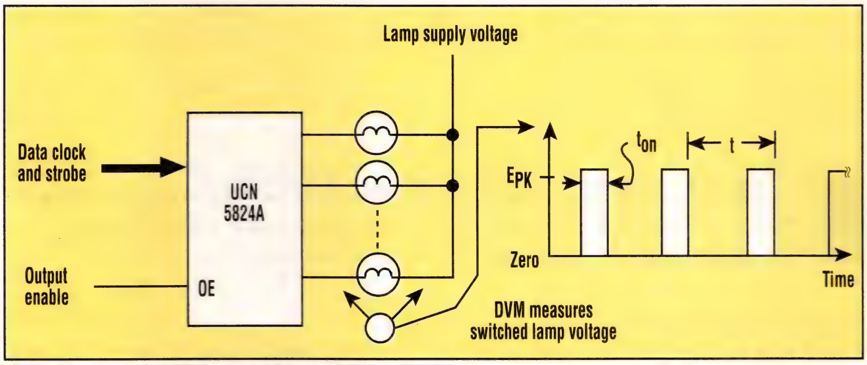
Power to resistance "R" during "t_{on}" = $E_{PK}{}^2/R$. Average power over full cycle time "t" = $E_{PK}{}^2/R \times t_{on}/t$.

Thus, by definition, power is $E_{rms}{}^2/R$. Therefore, $E_{rms}{}^2 = E_{PK}{}^2 \times t_{on}/t$ and $E_{rms} = E_{PK}(t_{on}/t)^{1/2}$. Average dc value $= E_{AV} = E_{PK} \times t_{on}/t$.

Therefore, $E_{rms} = E_{AV} \times t/t_{on} \times (t_{on}/t)^{1/2} = E_{AV}(t/t_{on})^{1/2}$, and $E_{rms} = E_{AV} \div (\text{duty cycle})^{1/2}$.

The true rms voltage thus equals the average dc voltage divided by the square root of the duty cycle.

Accuracy will depend on how closely the lamp waveform comes to being truly square. Ultimately, though, it won't be far off and virtually any dc voltmeter can be used for the measurement.□



BY SETTING A DISPLAY FOR ALL eights and obtaining a lamp drive waveform, any average dc responding voltmeter can be used to measure for and eventually attain true rms voltage.

IFD Winners

IFD Winner for June 24, 1993

Tunc Doluca, Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086; (408) 737-7600. His idea: *"Add Switch-Mode To Battery Charger."*

IFD Winner for July 8, 1993

Patrick Garner, Advanced Technology Systems, 800 Follin Lane, Vienna, VA 22180; (703) 242-0030. His idea: *"Function Generator Uses +5V, Ground."*

Send in Your Ideas for Design

Address your Ideas-for-Design submissions to Richard Nass, Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

CIRCLE 522

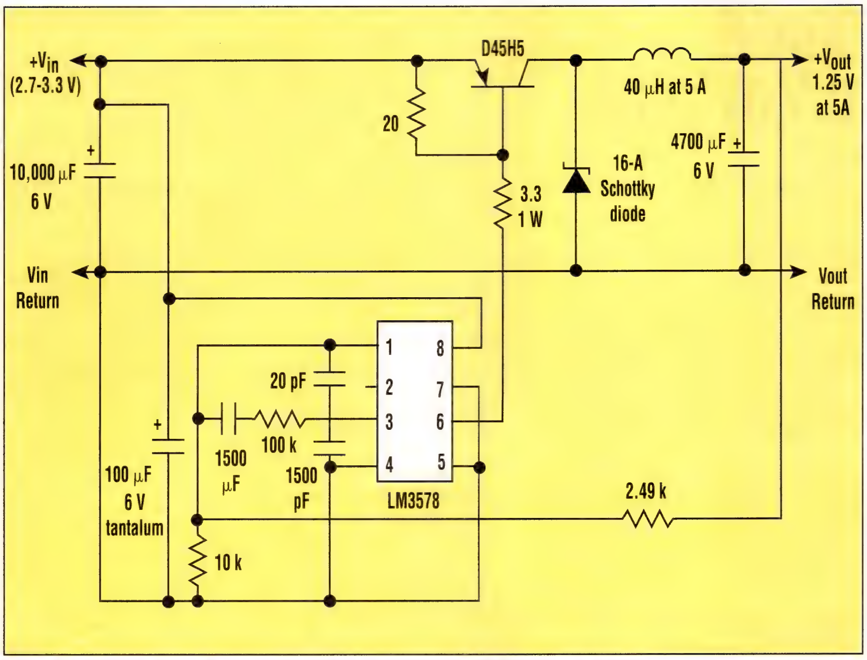
Switching IC Runs From 2.7-V Input

CHESTER SIMPSON
National Semiconductor Corp., M/S-C2503, P.O. Box 58090, Santa Clara, Calif. 95052-8090; (408) 721-7501, fax (408) 721-7321.

The rapid proliferation of 3-V logic systems is generating requirements for circuits that operate from supply voltages as low as 2.7 V. The device shown here *(Fig. 1)* underscores that point, as it was devised in response to a customer request for a 1.25-V "bus-termination" voltage in a system that was powered from a 3-V main power bus. This step-down (buck) switching regulator will provide a regulated 1.25 V at 5 A from a 2.7-to-3.3-V input.

When trying to come up with a solution to the customer's request, it became clear that the minimum input supply voltage of 2.7 V was too limiting of a constraint for power FETs: There are no power FETs that can be fully turned on with only 2.7 V. This meant that FETs couldn't be used without some kind of internal converter to generate a higher voltage to drive the gates (this was eventually ruled out because of additional circuitry and cost).

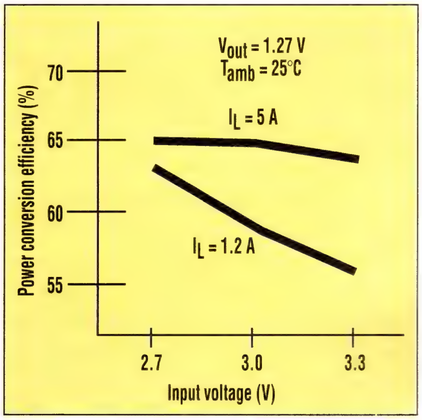
As an alternative, the device in Figure 1 was designed. It uses a single fast-switching pnp transistor (type D45H5) driven by an LM3578 controller (selected because it will operate on voltages as low as 2 V and it provides up to 750 mA of drive for the pnp). A 16-A Schottky diode (TO-220 package) was used for the output



1. THIS STEP-DOWN SWITCHING REGULATOR provides a regulated 1.25 V at 5 A from a 2.7-to-3.3-V input. Key to the design is the use of a single 8-A fast-switching pnp transistor, which is driven by an LM3578 controller.

diode to minimize power loss (an 8-A diode can be used with an efficiency loss of about 3% at a 5-A load). No heat sink is required.

Looking more closely at the circuit design, the LM3578 is connected in the basic step-down configuration, with component values selected for a 1.25-V output and 40-kHz switching frequency. The 8-A D45H5 has good saturation current at 5 A and low switching losses at the 40-kHz operating frequency. Only a small heat sink is required, as the power dissipation was less than 3 W (worst case).



2. EFFICIENCY results for the switching regulator are shown in this plot. The efficiency, defined as P_{load}/P_{in}, was approximately 65%.

The toroidal-type inductor is recommended for the output filter because it produces less EMI noise. The input and output capacitors must be aluminum electrolytics with very low equivalent series resistance (ESR). In the breadboard unit, Panasonic HFQ-type capacitors were employed.

Generally, good power-conversion efficiency in a switching converter requires that the voltage drops (and power dissipation) associated with the switching devices be very small when compared to the output voltage (and power delivered to the load). However, for this buck regulator, the 1.25-V output voltage means that the voltage drops across the pnp switching transistor and the output diode aren't negligible. In fact, they're quite significant.

To minimize power dissipated in the switching transistor, a single pnp was used (as opposed to a pnp/npn Darlington combination). If sufficient base drive is provided to the pnp, it can be pulled hard enough into saturation to force its collector-emitter voltage well below 1 V. This keeps the "on time" power losses as low as possible.

The following results were obtained with the device: load regulation = 0.45% (V_{in} = 3 V, I_L = 1.2 A – 5 A); line regulation = 0.32% (I_L = 5 A, V_{in} = 2.7 V – 3.3 V); output noise (rms) = 1.28 mV (V_{in} = 3 V, I_L = 5 A, Fluke 8050A).

The circuit efficiency (defined as the ratio P_{load}/P_{in}) was about 65% at a 5-A load, and is essentially independent of input voltage at that current level *(Fig. 2)*.☐

CIRCLE 523

BUILD AUTOMATIC TAP CHANGER

GEOFF DRUMMOND
Advanced Energy Industries, 1825 Sharp Point Dr., Fort Collins, CO 80525.

The automatic tap changer comes in handy when automatically adjusting for large line variations seen from poorly regulated line power. It's also useful when automatically adjusting for small differences in line power ranges that occur from country to country (100/115 V ac or 200/230 V ac, Japan/U.S.). The circuit discussed here is intended for new equipment possessing electromechanical components (ac motors, high CFM fans), as well as linear or unregulated power supplies. It can also be packaged separately and used as a line conditioner on to existing equipment to improve performance and life.

An automatic tap changer can be particularly effective when it comes to ac fans. Some ac fan manufacturers report that operating a fan more than 5% above its nominal ac rating can decrease fan life as much as 50%. Running an ac fan too far below its nominal rating can significantly reduce its CFM output, causing unnecessary heating in the components that it's cooling. With this circuit, however, line variations to the load are cut in half, optimizing life and

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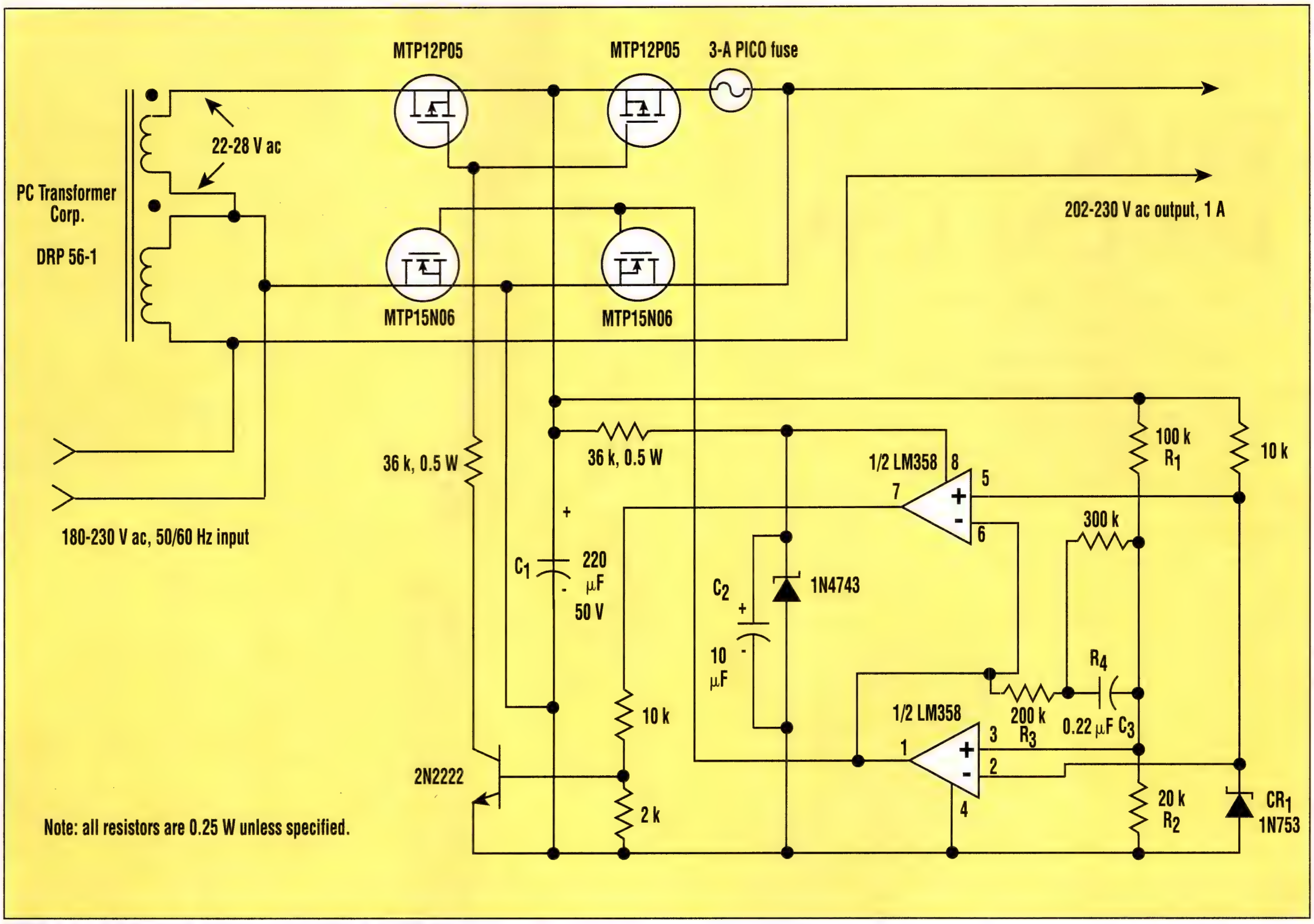

AN AUTOMATIC TAP CHANGER is beneficial when it comes to automatically adjusting for large line variations seen from poorly regulated line power. The simple circuit's main components are two electronic ac switches and a control circuit.

performance *(see the figure)*. The device reduces the heat dissipation on the series pass element of linear supplies. And in some less demanding applications, with the regulation the tap changer provides, a series regulator can be eliminated.

Simplicity defines the circuit: Its fundamental components are two electronic ac switches and a control circuit that decides when a tap change is necessary *(see the figure, again)*. Each ac switch consists of two VMOS transistors connected in series, with their sources forming a common node. The control circuit is powered from the ac voltage difference that's developed between the two tap positions. This ac voltage is rectified by the intrinsic diodes present in each VMOS transistor pair that form each switch. That's one reason why one switch uses a p-channel pair and the other employs an n-channel pair. The rectified voltage is filtered by C_1. Because C_1's dc voltage level is proportional to the input line voltage, it's used to determine the input line voltage threshold at which to change taps.

The LM358 in the circuit has two op amps in one package. One op amp acts as a comparator, the other as an inverter. R_1 and R_2 along with CR_1 determine the line voltage threshold to change taps. C_3 and R_3 are used for the hysteresis that's necessary to keep the circuit from continuously changing taps when the input line is at the threshold voltage. The device's auto-transformer was built by properly phasing an isolation transformer. An auto-transformer with a 10% tap is quite small when compared to the power it's supplying (a 10-VA transformer can be used for a 100-VA load).

Although the circuit shown has two discrete tap ranges, it can be extended to include more taps. Another variation could have a smoothing inductor and high-frequency (PWM style) operation to maintain a well-regulated output voltage.☐

Guidelines on Length for Ideas for Design Submissions

Space is limited in the Ideas for Design section. Many submissions are returned to the authors simply because they are too long or require too many illustrations.

The ideal length is between one and two double-spaced typed pages with just one illustration.

If a second illustration is required, it should be substantially smaller than the primary diagram. Oscilloscope photos can be included if they show results, but be sure to include voltage and time scale settings.

If the idea is accepted, we will edit it and return a copy to the author for a final technical accuracy check before publication. We will redraw all diagrams to conform to our style.

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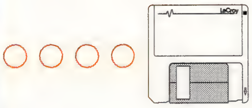

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CIRCLE 135 FOR RESPONSE OUTSIDE THE U.S.

BOB'S MAILBOX

Dear Bob:

I was just finishing up a report on fuzzy logic when a co-worker handed me a copy of your article "What's All This Fuzzy Logic Stuff, Anyhow?" in the May 13 issue. In short, I agree. It is extremely refreshing to hear a voice of reason in this age of emperor's new clothing.

I have included the first version of said report. It covers the development of a fuzzy-logic controller (and that of a corresponding classical controller) for the balancing of an inverted pendulum attached to the end of a robotic arm. The effort was requested by NASA in order to aid in the evaluation of fuzzy-logic-control-system design techniques. I hope you can find time to read it (at least the results and conclusions).

In the article, the use of the term "deterministic" to describe conventional controllers is unfortunate because it implies that fuzzy-logic controllers are not deterministic. In fact, fuzzy-logic controllers are completely deterministic. More specifically, the end result of a fuzzy-logic control system (assuming no add-ons or hybrids) is simply a function. That is to say, it generates a unique value of any output variable (e.g. current to a motor) for every unique set of values on the input variables (e.g. angular position and rate of the motor shaft as feedback variables).

Fuzzy logic is simply a design technique that is based on the use of intuition in designing a control function—a method to convert fuzzy human statements about how to control something into a completely deterministic relationship between controller inputs and outputs. Now, any control function can be developed in many different ways (a linear function can even be easily modified to be nonlinear *if* desired, what with today's modern computers!), and the performance is only dependent on the function, not the technique used to develop it. Thus the *real* issue is whether one technique or another is more helpful to the designer in developing a function. What technique(s) is used is primarily a matter of taste for the designer. Statements such as "fuzzy-logic controllers perform better than conventional controllers" are nonsense.

Finally, let me say that the idea of using fuzzy logic to convert human intuitive statements into a working function initially caught my fancy (for various reasons). However, this is far more complicated than it sounds. In my development of two very different control systems (one being a highly nonlinear "phase plane" controller for thruster-actuated space vehicles) with fuzzy logic and other control techniques, fuzzy logic proved to be a very poor technique. It took me *far* longer to develop fuzzy-logic systems, that achieved the same performance (and almost identical resulting functions) as with the other techniques that I used. The designer must mentally juggle many numbers and rules in specifying the fuzzy-logic system, and understanding the relationships between these and the observed system behaviors can be very frustrating indeed.

LAWRENCE E. MERKEL
Lockheed-ESC
Houston, Texas

Isn't it funny—the F.L. approach is always very easy for F.L. guys who don't know how to do it any other way! I suspect that making F.L. work well isn't as simple as they say. Thanks for your observations.—RAP

Dear Bob:

I recently read an article that talked about the lack of "feel" for engineering in the current crop of engineering students. It disturbed me that this condition should exist. The article goes on to lament that many of the students had never dissected nor constructed anything before graduation, and that special courses were being designed for this purpose. What in the world are they doing in the field if they have gotten as far as college and have not dissected anything or constructed anything?

When I was nine years old, I constructed my "soap box" racer out of an old crate, a 2-by-4, and a roller skate that I had taken apart. I even had a headlight that I had made from the lens/bulb assembly of an old flashlight and a large type "A" cell. I did all this without any input from adults. I copied the design from "soap box" racers that I had seen kids use in Brooklyn, N.Y.

In 1955, when I was in the 8th grade, I got an "Honorable Mention" for my science fair exhibit, "The Transistor, an Electronic Marvel." I constructed a two-transistor audio amplifier (using Raytheon CK722s) and explained its operation and the operation of the transistor. I suppose it really was an engineering project and not scientific research. I did it on my own initiative and without any adult guidance. Maybe I would have done better if I had some guidance, but maybe it would not have served me well in life.

As a fifteen year old, I built a shortwave converter for my AM radio. I got the circuit schematic from an amateur radio handbook. I purchased the components, did the sheet metal work, and assembled it by myself. There was no adult involvement here either. I still have it and it still works.

I don't know if you are familiar with the famous "Canal Street" in New York City. At least it was famous in the '50s for its surplus electronics outlets. I used to make many pilgrimages there in my youth. On one trip, a friend and I carried home a 400-Hz generator "safari style," i.e., slung from a pole we carried between us on our shoulders. He needed it for his surplus ham equipment. We carried it this way on the Staten Island Ferry and then onto the New Jersey Central Railroad for the ride home. I had picked up a bargain mercury thermometer, which promptly got broken when I got caught in a swinging door at the ferry terminal. Ouch, a whole buck down the tubes....

The examples I could cite are almost endless. You may say that my experience was unique. Well, at the time it wasn't. Most of the people I knew in the College of Engineering at Rutgers University were either hams or hobbyists or experimenters. I, and others in my lab group, could not believe it when one of our lab partners asked us what a resistor looked like. He had done all the theoretical calculations in the various classes, but had never actually handled any of the parts. He was unique, though, and caught on quickly. He later got his PhD in Physics and was doing heat balance work on communications satellites.

You may say that kids today don't do that kind of thing anymore. Well, you would be wrong. My son, who's a junior in high school, worked on robotics projects at home during the summer. He has an old VIC-20 computer and a Fischer-Techniks kit. He is building working models of machine tools and other gadgets. He has assembled a siren, an AM radio, a burglar alarm, model rockets, and other goodies from kits. He has taken "junk" electronics and made them functional. He has dissected countless mechanical gadgets. He works on his bicycle by himself. He has the "soul" of an engineer. I think it comes from within. I don't think you can train it into someone.

So, tell me what is really wrong with today's crop of engineers? Is it the age of instant gratification, where building a kit model airplane takes too long? Is it the lack of role models? After all, anyone today who likes math and science is considered a nerd. In my day, I was classified as an "egghead." But I got along with everyone: jocks, hoods, and the "in" crowd. I did not consider it a "put down." How would I fare today?

Finally, I am appalled that the article states, "Employers visiting the campus stress that it is more their communication skills that help students advance than engineering know how." I suppose you can design junk, but as long as you present it well, it's OK. I wonder if you value communications skills over engineering skills?

Why am I rambling on like this? Well, I feel that you are a kindred soul. You, and others like you, seem to be a breed that is slowly dying out. Any comments?

ALEXANDER F. JASZEK
Needham, Mass.

Well, since most electronic stuff is "non-repairable," and there are no more Heathkits, it's hard to get kids interested in electronics—unless you count computers. There are still some bright kids coming along. Maybe we don't need more engineers, but we could sure use some smart ones!—RAP

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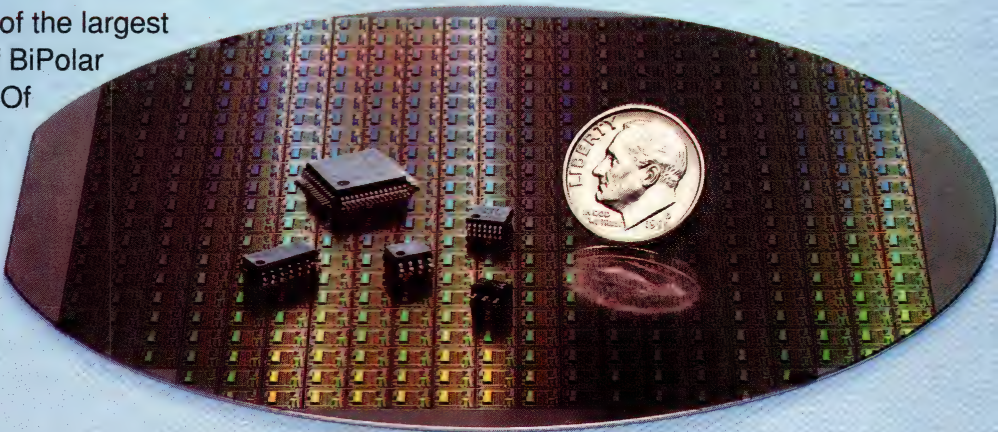

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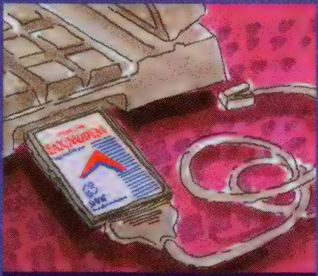

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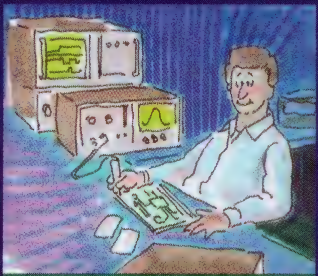

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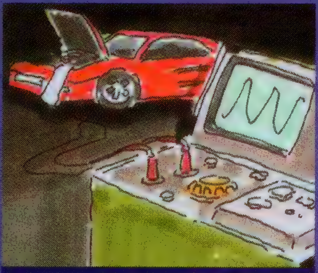

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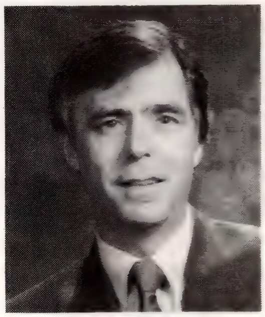
PLUGGING INTO PCMCIA

COMMUNICATIONS ON THE GO

JOHN HUGGINS, TDK SYSTEMS DEVELOPMENT CENTER

Portability has become a dominant technology driver for the PC industry. Innovations have created portable machines that emulate, and in the case of interchangeable PCMCIA cards, extend the capabilities of the desktop. However, portable computing suffers from one major limitation: communications. PCMCIA-based modems are now widely available, making home- or hotel-to-office communications possible. But, truly mobile users need "communications on the go." This concept means communications must be possible from a dispatched vehicle, an airplane, a remote monitoring site, etc. These communications will be carried over the airways, and the physical connection to the computer will disappear. Wireless PCMCIA cards will dominate the format of these products.



Several obstacles must be overcome before widespread wireless communications can become a reality. These include available services and infrastructure; transmission standards and frequency allocations; transceiver miniaturization; better power management; and uniform applications drivers that make the services easy, if not transparent, for the user.

The infrastructure for airborne services already exists in several forms: radio-borne pagers, private-radio packet data services, and wireless LAN (WLAN) technologies. PCMCIA cards supporting most of these services have been shown or announced within the past year.

Early products have been limited to vertical or closed applications. Ubiquitous user-to-user applications will probably be carried on private data radio or public cellular networks. Such networks, both in the U.S. and Europe, are moving rapidly to implement a switched or packet data-channel capability. PCMCIA cards will be quick to follow the service offerings, provided some power problems can be worked out.

Wireless standards are further encumbered by regulated frequency allocations. Current options in the U.S. include an "Emerging Technologies" band, and three unlicensed "Industrial, Scientific, and Medical" (ISM) bands. There are also licensed data radio and cellular bands. The International Radio Consultive Committee has been attempting to harmonize national frequency standards to allow the possibility of marketing and using products across international boundaries.

PCMCIA technical committees recently reviewed proposals pertaining to connectors for wireless PCMCIA communications cards. There's no provision in the current standard (Release 2.01) for conducted RF or IF (intermediate frequency) signal transmission between the host and the card. Therefore, a host-based printed antenna can't be connected to RF transceivers residing in the PCMCIA card. That's unfortunate, because printing the internal antennae and housing it in the host enclosure forms a low-cost solution. In addition, the antennae could also be replicated orthogonally for better directionality, a feature difficult to achieve in an inconspicuous, external design.

The disadvantage of integrated host antennae is that they're optimized for one carrier frequency and different applications require different frequencies. In addition, the same materials used in the enclosure plastics to provide RFI shielding will attenuate the transmitted and received RF signals, typically by 12 dB. One PCMCIA proposal allows alternate connection to an external antenna, which could be provided as part of the PCMCIA card.

Miniaturized transceivers have been demonstrated in the PCMCIA-card format for IR and RF wireless approaches. Further advances in magnetics and materials, such as low-profile shielded surface-mount multilayer R-L-C networks for RF, are making PCMCIA implementations even more feasible and economical. IC technologies, particularly analog-optimized BiCMOS and gallium arsenide, are reducing component count and unifying system approaches at the chip-set level. These trends will make wireless cards less expensive and more popular.

Another potential problem is the large amount of power required for transmission. Few 3.3-V notebook computers, and virtually no handheld hosts, can supply the cellular-class power (2 W). In pagers, power denial by the host during a sleep mode could deactivate the receiver automatically, resulting in an unintentional reception loss. PCMCIA Card Information Structures (CISs) offer a means for cards to relay their capabilities and requirements to the host in a uniform manner. With the CISs, host processes can adapt to the particulars of the card using card and socket services as well as application-software clients. Thus, the PCMCIA is looking to adopt similar uniform CIS tuples for common wireless cards.

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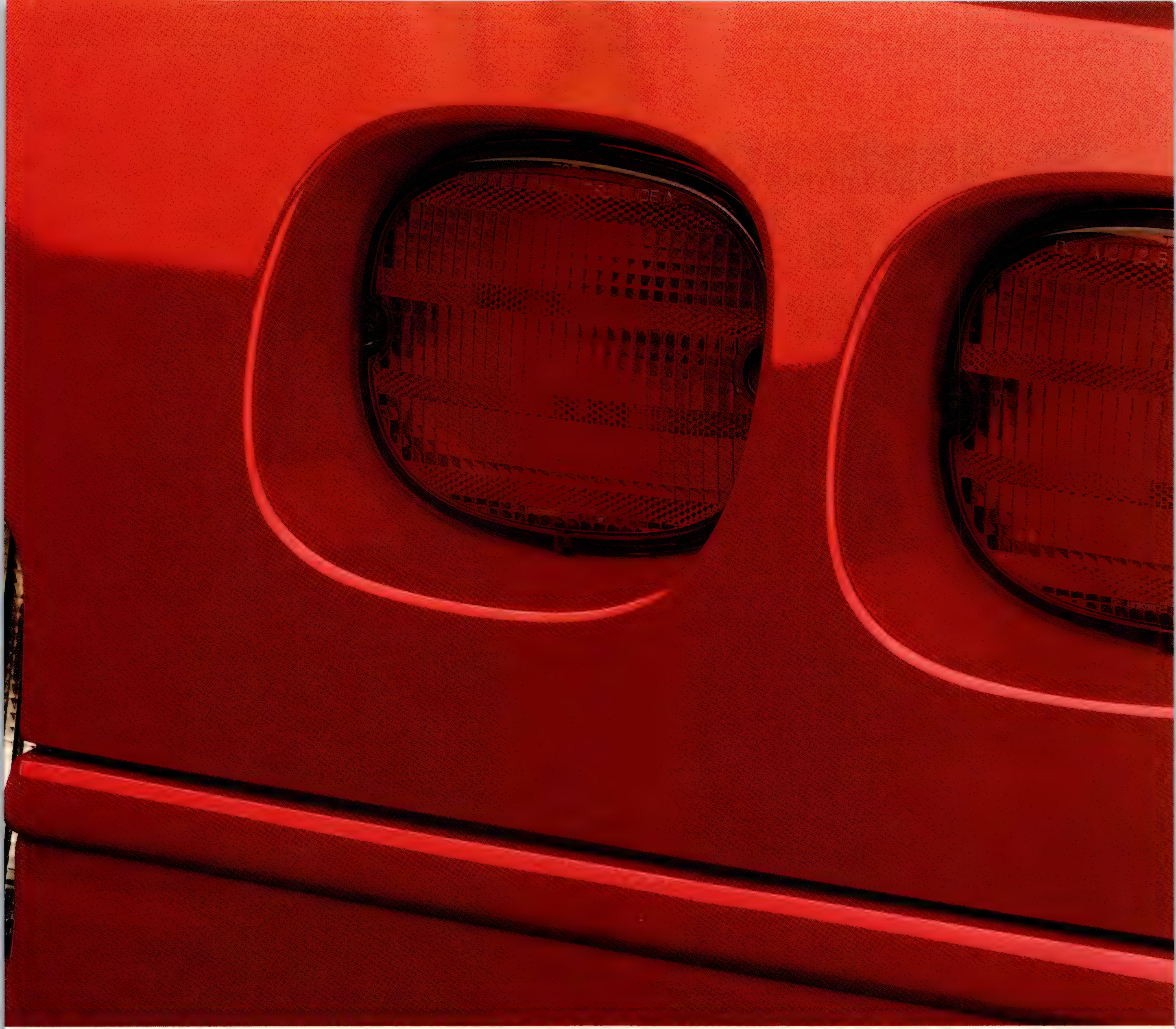

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CIRCLE 127 FOR RESPONSE OUTSIDE THE U.S.

An Application Model Points To The Right Controller

Modeling an embedded application helps designers choose a microcontroller based its features.

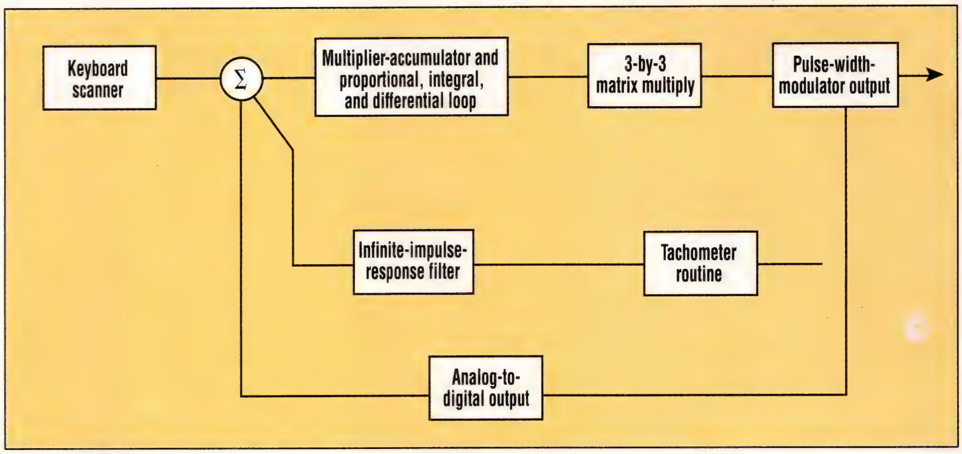
BY STEVEN MCINTYRE

Intel Corp. 5000 W. Chandler Blvd., Chandler, AZ; (602) 554-8051.

How do engineers select microcontrollers for embedded applications? Ideally, they should carefully weigh the technical merits of each architecture in the context of their application. But, unfortunately, that's not always the way it's done. Instead they use a mixed bag of methods that may or may not result in the optimum choice of microcontroller. Thus, the most effective method is to begin with a model of the application's key characteristics and use this to select the microcontroller.

In large corporations, selection is generally done by architecture evaluation groups that are chartered to investigate microcontrollers for their technical/business merits. They tend to look for all of the important ingredients: development tools, price/performance matching to an application or market and application-specific I/O performance, and other similar criteria. While this is a strongly structured method of product selection, it tends to be costly. Moreover, such groups can have short lifetimes: they're often downsized or even eliminated during rough business cycles, and the decision is placed back on the engineer's shoulders.

One common decision-making method is to sketch out a model of the application, check what the application will need to do, and then attempt to match those functions to a microcontrollers' features. The engineer would typically refer to a semiconductor manufacturer's line card, which has the microcontrollers' features listed in tabular form for easy reading.


Keyboard scanner
Σ
Multiplier-accumulator and proportional, integral, and differential loop
3-by-3 matrix multiply
Pulse-width-modulator output
Infinite-impulse-response filter
Tachometer routine
Analog-to-digital output

1. A typical embedded-control application usually requires analog-to-digital sampling; pulse-width-modulation signals; a tachometer routine to measure motor or power-plant output response; digital filtering; and a proportional, integral, and differential control loop.

But, for all of the line card's usefulness, it doesn't give you the full picture. For example, it might show a column for serial ports. If the application requires three serial ports and the device supports only two, does this mean that the device isn't suitable? Not necessarily, because the engineer may be able to emulate a serial port using other I/O. Moreover, what about the performance impact if a serial port is emulated using general I/O? What would be the highest baud rate? This type of application-specific peripheral information, though important, is generally not listed in line cards.

Another way engineers pick microcontrollers is familiarity. They simply choose a device that they've used before—not for its cost effectiveness, technical merit, or low-cost development tools. The fast pace of the high-technology industry often presses engineers to complete a project as quickly as possible, and learning a new processor would take more time than they have. On the other hand, engineers often don't know how much CPU performance, I/O, or other functions they will require, so they choose the newest, fastest device. This isn't always appropriate, because mature technologies have already gone through their learning curves and tweaked out anomalies that might plague newer devices.

A better way to select a microcontroller is to model the system in question. Engineers would then write software routines that represent the critical performance criteria of the model and weigh the merits of each microcontroller versus these requirements. However, this usually means that the engineer must read the microcontroller manual and manually tabulate each line of code for these routines by hand, which is a long process.

Because every microcontroller application is different in terms of resources required, there are no "standard benchmarks" that would apply across the board. However, some tools can be created to assist in the modeling of microcontrollers in an application. Most microcontroller manufacturers will be glad to take the engineers' code and model it for them. Engineers need to "test drive" a microcontroller for themselves before investing more time and money into a possible design solution (when was the last time a car was sold based on the salesman's word that he drove it and it ran fine?).

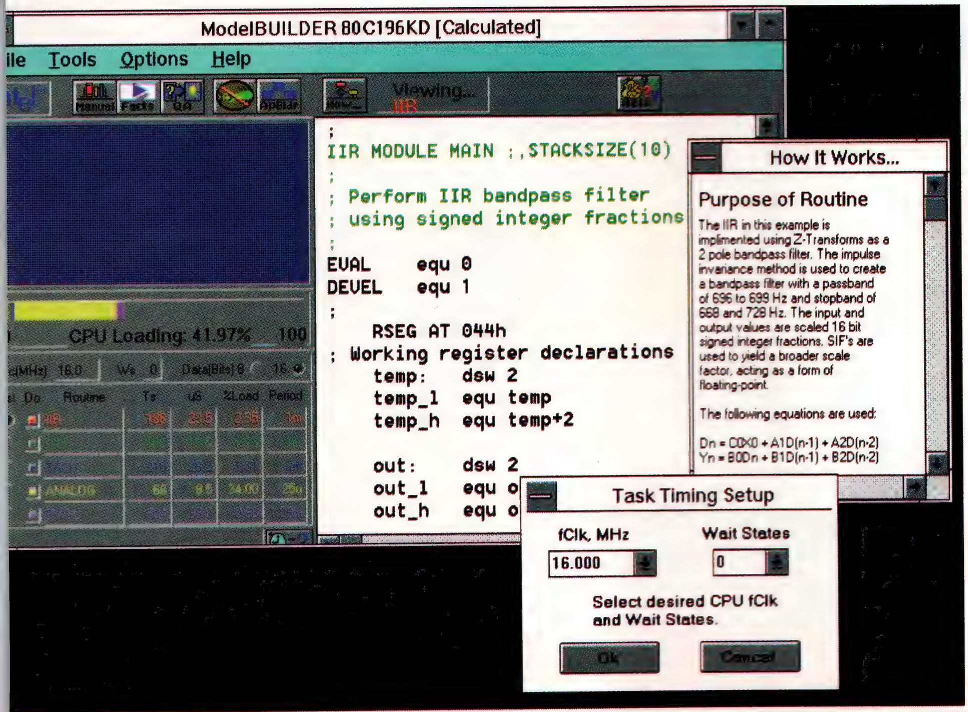
To understand what tools are required for modeling the system-level performance needed for an application, the engineer first needs to understand a typical embedded-control application *(Fig. 1)*. Such systems usually require analog-to-digital sampling to measure feedback and other inputs, a three-phase motor control or pulse-width-modulation signals to drive the system, and a tachometer routine to measure motor or power-plant output response. It would also need a digital filtering of these analog and digital signals, and a proportional, integral, and differential control loop to tie it all together.

To model the system-level performance of a microcontroller in the application, engineers would figure out which software routines (templates) would be combined into a model of the application. Typically, the selected routines are either the most difficult, the ones executed most often, or the ones requiring specialized software for deficiencies in I/O (as in the serial port example). They would then figure out how often these templates would be executed, based on the best-case/worst-case application requirements.

In some cases, the system can be modeled without understanding the microcontroller's details, such as when using a tool like Intel's ModelBUILDER. Preprogrammed performance templates exist for several 16-bit microcontrollers, including the 8XC196 family. These templates, which are the most common embedded-system building blocks used in event control, can be brought together through the click of a mouse. Within ten minutes, engineers can see the device's true performance (within 5%) in an application, and then decide whether it's worth a full evaluation.

An engineer can use the mouse to select from the list of preprogrammed performance templates in any combination to create a software model of the application. The designer then checks the device performance at different frequencies, bus widths, wait states, and different repetition rates to see how these parameters affect the microcontroller's overall performance. The tool requires neither prior knowledge of the device, learning the software model, nor figuring out how the device performs complex functions.

In a design example, an 80C196KD device running at 16 MHz with zero wait states and a 16-bit bus would require about 42% of the entire CPU processing power available *(Fig. 2)*. The designer can then check it at different performance template repetition rates (periods) or at different processor frequencies.



```
;
IIR MODULE MAIN ;,STACKSIZE(10)
;
; Perform IIR bandpass filter
; using signed integer fractions
;
EVAL     equ 0
DEVEL    equ 1
;
   RSEG AT 044h
; Working register declarations
   temp:    dsw 2
   temp_l   equ temp
   temp_h   equ temp+2

   out:     dsw 2
   out_l    equ o
   out_h    equ o
```

Purpose of Routine

The IIR in this example is implmented using Z-Transforms as a 2 pole bandpass filter. The impulse invariance method is used to create a bandpass filter with a passband of 696 to 699 Hz and stopband of 668 and 728 Hz. The input and output values are scaled 16 bit signed integer fractions. SIF's are used to yield a broader scale factor, acting as a form of floating-point.

The following equations are used:

Dn = C0X0 + A1D(n-1) + A2D(n-2)
Yn = B0Dn + B1D(n-1) + B2D(n-2)

fClk, MHz: 16.000
Wait States: 0

Select desired CPU fClk and Wait States.

2. Using the ModelBuilder software, designers can check the performance of a microcontroller at different performance template repetition rates (periods) or at different frequencies. In this example, an 80C196KD device, running at 16 MHz with zero wait states across a 16-bit bus, would require about 42% of the CPU's available processing power.

There are cases when engineers wish to write their own routines and download them to real target systems to check device performance. Using a kit called ProjectBUILDER, this task can be done on their own code. ProjectBUILDER takes the ModelBUILDER software and runs it on a target board with a retargetable symbolic debug monitor and an assembler. With this kit, engineers can build their own performance templates and test drive the device for themselves.

Creating performance templates still requires knowledge of the microcontroller. With this technology and other software tools like it, engineers may someday soon create customized system models without any prior knowledge of a proprietary microcontroller.

Steven M. Mc Intyre, applications manager at Intel Corp.'s Embedded Microcomputer Div., received a BS in computer science from Northern Arizona Univ., Flagstaff.

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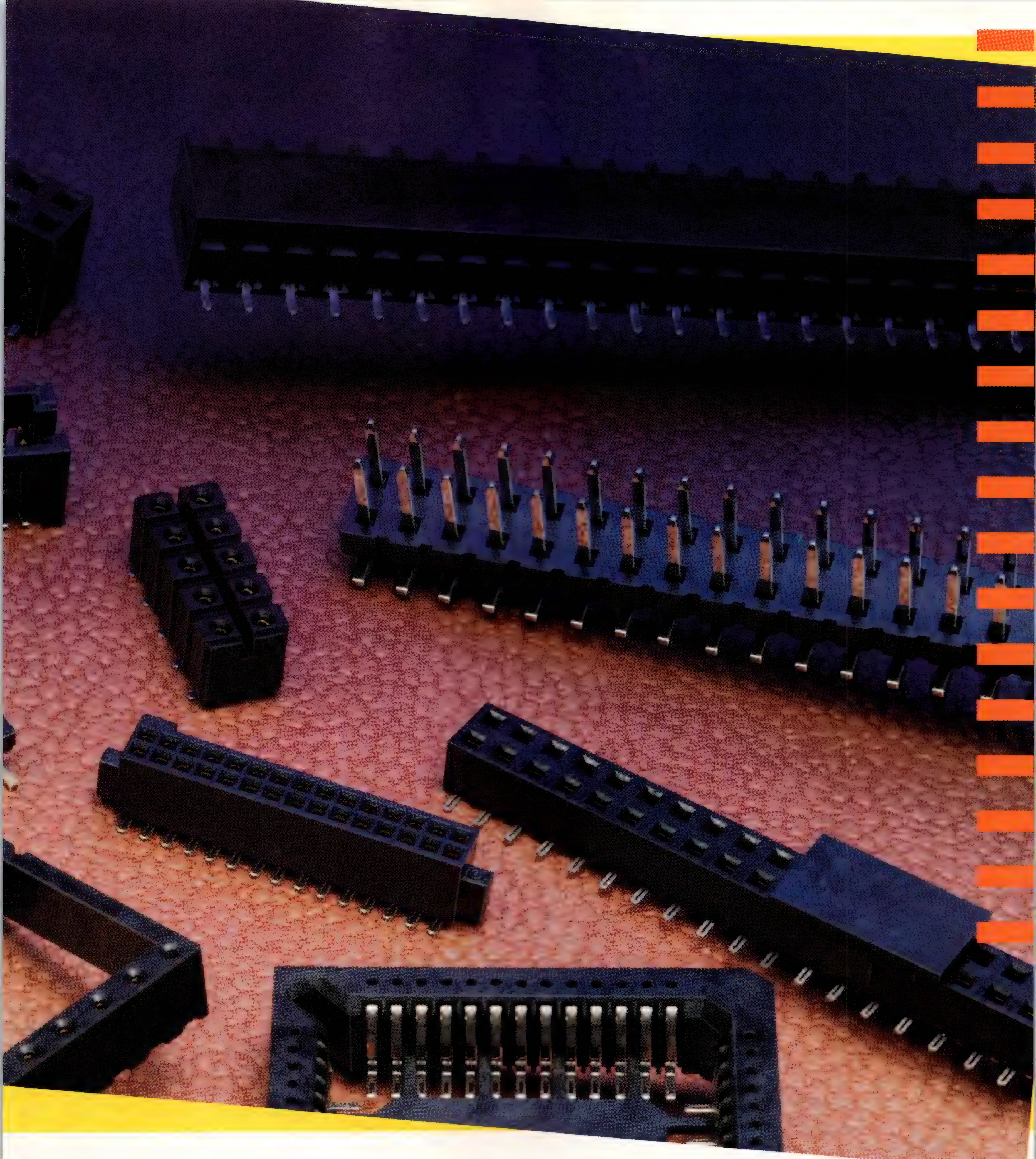

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SYSTEM DESIGN NEWS

With an on-chip clock doubler and a 16-bit pixel port, the STG1700 color palette DAC improves the transfer rate from new VGA controllers that also offer 16-bit pixel ports, while simplifying system design. Wide pixel ports are currently available on controllers such as the ATI 68800AX, the S3 805i, and the Tseng 4000/W32P. The clock doubler embedded by SGS-Thomson Microelectronics Inc., Carrollton, Texas, reduces the external frequency requirements from 135 MHz to half that value. Thus, it's easier to generate system clocks, and less noise is radiated. In addition, this mode offers an ISO-compatible, 256-color, flicker-free display with up to 1280 by 1024 pixels at a refresh rate of 75 Hz. Also supported are 1024-by-768-pixel and 800-by-600-pixel modes with 65,000 and 16.7 million colors, respectively. The 44-pin, PLCC-housed palette DAC is backwards-compatible with the 44-lead pinout of the standard 8-bit pixel-port palette DACs. The STG1700 also includes the company's PixMix feature, which allows the user to switch between pseudo and direct color on the same screen on a pixel-by-pixel basis. Just coming out of development is a second palette DAC, the STG1702, which offers enhanced true-color performance thanks to a double, 24-bit, packed-pixel mode available on a serializing 16-bit pixel port. Samples of the STG1700 are immediately available. In volume purchases, the device sells for less than $10 each. For more information, contact Peter Lobo at (214) 466-6000.

A PCMCIA fax/modem card adds voice communications capabilities, making it possible to voice-annotate documents, transfer multimedia presentations, handle voice e-mail, perform remote access of personal voice and fax messages, and perform other voice-related applications. The Mercury Card designed by MagicRAM Inc., Los Angeles, Calif., slides into PCMCIA type II or type III slots and comes with voice-enabling software—SuperVoice 1.0—for either Windows or DOS environments. The SuperVoice software manages multiple voice mailboxes, handles incoming faxes, automatically switches to voice calls, and allows voice annotation of Windows or DOS applications. The card's fax/modem portion supports Group 3 fax transfers at up to 9600 bits/s (CCITT V.29). The modem portion supports the "AT" command set while operating at up to 2400 bits/s (CCITT V.22 bis). To conserve system power, the card also includes an automatic power-down mode that trims the 100-mA operating current to just 22 mA during inactive periods. Designers at the company were able to embed the data-access-arrangement (DAA) circuitry in the card, rather than keep it external to the card like most other fax/modem card manufacturers. Just a simple "Y" connector plugs into the card. One top leg of the Y goes to the telephone line, while the other top leg connects to a telephone handset, which serves as the microphone and speaker. The card will initially sell for $245 each. For more information, contact Alan Nouray at (213) 413-9999.

A conference focusing on the development of the "Common Desktop Environment" (CDE) will present both general information and technical sessions to provide attendees with an in-depth view of CDE. Presentations will focus on CDE integration, product strategy and direction, end-user benefits, and CDE's potential impact on the open-systems industry as a whole. Scheduled for October 26-28 at the San Jose Convention Center in California, the conference will be hosted by the Uniforum Association, Santa Clara, Calif., and the engineers involved in creating the CDE specification (they're currently building a CDE sample implementation). A pre-conference tutorial will cover the core component of CDE—the Open Software Foundation's Motif Toolkit and Window Manager. In addition to the conference proceedings, attendees of the conference will also receive sample implementation code for the Intel, IBM, HP, and Sun platforms on CD ROM. For registration details, contact Richard Jaross at (408) 986-8840 or by Internet e-mail: rich@uniforum.org.

▼ PCMCIA HARD DRIVES PACK UP TO 170 MBYTES

Portable computers built with PCMCIA slots can utilize all available PCMCIA-based peripherals. So far, most of those peripherals have consisted of solid-state memory and communications devices. Rotating storage has been around for some time, but the available capacities limited the applications. Now, thanks to the Viper series of drives, users can plug up to 170 Mbytes into their Type 3 PCMCIA slots.

The two available models, the 105-Mbyte 8105PA and the 170-Mbyte 8170PA, are two-platter, four-head drives that feature 15-ms access times. They can absorb 500 Gs of non-operating shock and 100 Gs while operating. Using programmable power-management functions, the drives spin up in 1 second from a 25-mW sleep mode. They also incorporate a dynamic head-loading feature that keeps the heads from coming in contact with the disk surface, thus protecting the head-disk interface. The 8105PA will be available in November for $495. It will also be bundled with software and a carrying case as an end-user product, called the PocketFile 105. The cost is $750. The 8170PA, available in the second quarter, will sell for $595.

Integral Peripherals Inc.
5775 Flatiron Pkwy.
Boulder, CO 80301
(303) 449-8009
▶ CIRCLE 585

▼ REMOVABLE DRIVES STORE UP TO 360 MBYTES

The K-Stor 0.5-in.-high removable hard-disk drive kit comes in capacities of 250 and 360 Mbytes. The kit contains the drive, a docking module, software, and a carrying case. The docking module, which fits into a standard 5.25-in. half-height drive bay, allows users to insert the drive into a system. With additional modules, the drive can be plugged into multiple systems. The 250-Mbyte K-Stor drive kit sells for $495, while the 360-Mbyte model costs $595. Additional modules are priced at $100.

Kalok Corp.
1289 Anvilwood Ave.
Sunnyvale, CA 94089
(408) 747-1315
▶ CIRCLE 586

▼ REMOTE MOUSE IS MICROSOFT COMPATIBLE

The LaserMouse, intended for multimedia applications (including presentations), is a remote pointing device that offers full Microsoft-mouse compatibility. The device looks like a conventional television remote control, but has the combined capabilities of a mouse and a standard PC/AT keyboard. With the LaserMouse, the user can wander around a room while maintaining complete control of a Windows environment. The device is available now in three configurations.

TV Interactive Corp.
1546 Centre Pointe Dr.
Milpitas, CA 95035
(408) 946-2417
▶ **CIRCLE 587**

▼ FUNCTIONALLY TEST PCMCIA CARDS

Targeted at manufacturers and designers of PCMCIA devices, the FT-20x series of functional testers can support both military and commercial projects. The testers are suited for design verification, production testing, and incoming and outgoing inspection.

The FT-201, the first in the series, is a single-board system that supplies a dual-socket interface, but occupies just one 16-bit expansion slot in a PC's backplane. It will functionally verify for compliance either one Type III or two Type I or II PCMCIA devices, including memory, I/O, or rotating disk drives. Multicard configurations are available for volume testing or burn-in. The tester comes bundled with a Microsoft Windows utility that includes device selections, single and repetitive tests, pass-fail data logging, and standard read-write capabilities for all memory technologies. The FT-201 sells for $1295 with large-quantity discounts available.

MSD3 Inc.
365 Woodview Ave. #700
Morgan Hill, CA 95037
(408) 778-7267
▶ **CIRCLE 588**

▼ PCMCIA FLASH CARDS HOLD UP TO 16 MBYTES

The CatFlash family of flash-memory cards, available in 512-kbyte and 1-, 2-, 4-, 8-, and 16-Mbyte capacities, all comply with the 68-pin Type I JEIDA and PCMCIA standards. Features include 120-ns access times, separate EEPROM attribute memories, and configurations for 8- or 16-bit-wide bus interfaces. The cards run from a –0.5- to +7.0-V supply. The active read current is 80 mA, while the write current is 60 mA. In standby mode, the cards consume 1.6 mA. The operating temperature ranges from 0 to 60°C. The 1-Mbyte card sells for $239 and the 2-Mbyte model costs $399. All members of the CatFlash line are available now except for the 16-Mbyte card, which is scheduled for introduction in the early part of 1994.

Catalyst Semiconductor Inc.
2231 Calle de Luna
Santa Clara, CA 95054
(408) 748-7700
▶ **CIRCLE 589**

▼ FLOPPY-DISK CONTROLLER SUITS MOST DRIVES

The MFDC floppy-disk controller is software-compatible with most standard drives, including PC and PS/2 systems. The hierarchical controller supports 8-, 5.25-, 3.5-, and 3-in. drives. It also offers extensions to support perpendicular-recording-mode drives, FIFO operation, and standby mode. Moreover, it can address more than 255 tracks.

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SW109KA0012F01	25	+9	0-2.78	50	±1%
SW110KA0012F01	25	+12	0-2.08	50	±1%
SW111KA0012F01	25	+15	0-1.67	50	±1%
SW112KA0012F01	25	+16	0-1.56	50	±1%
SW113KA0012F01	25	+24	0-1.05	50	±1%
SW201KA0012F01	25	+5, +12	0-4.0, 0-1.0	50, 100	±1%, ±5%
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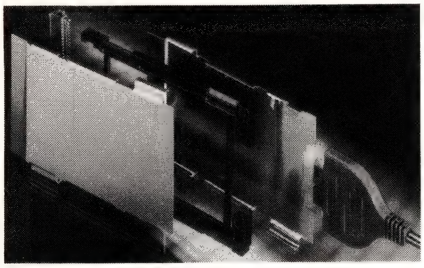
SYSTEM DESIGN PRODUCTS

▼ CONNECTOR SUPPORTS TYPE 2 PCMCIA CARDS

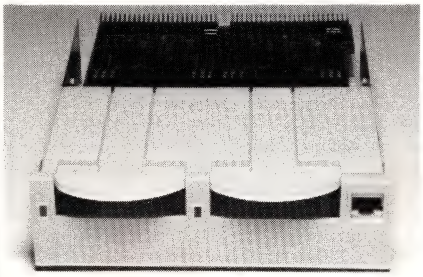
A newly released PCMCIA connector comes with the memory-card frame kit, a 68-pin header and receptacle assemblies, and I/O connectors. The connector, compatible with Type 2 cards, features dual spring-leaf contacts that are rated for up to 10,000 insertions. The connector is surface-mounted to a printed-circuit board and locks to the frame kit to increase reliability and to supply ground continuity. The mating plug connector, which is polarized to prevent mismatching, is available as a separate piece or as a cable assembly. The frame kit costs $1.87, the I/O receptacle is $1.80, and the I/O plug is $2.29, all in quantities of 25,000. The 68-pin mated-pair connectors sell for $6 each in quantities of 1000.



Amp Inc.
P.O. Box 3608
Harrisburg, PA 17105
(717) 564-0100
▶ **CIRCLE 591**

▼ PCMCIA CARDS PLUG INTO DESKTOP PCs

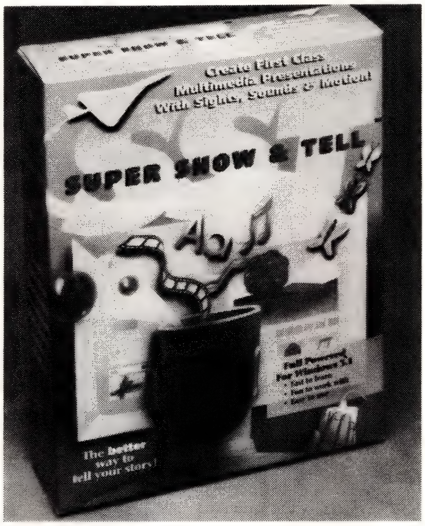
Fully compliant with all PCMCIA standards, the CardDock universal adapter enables easy plug-and-play of any memory or I/O cards. The device can read or write data, or exchange files between portable and desktop computers. The dual- or quad-slot system mounts in a standard 5.25-in. drive bay. Data loss or card damage resulting from power loss or accidental removal are reduced using a proprietary built-in sensor that automatically notifies the host to suspend an operation. The CardDock's software manages system resources with pop-up menus. The dual-slot system (GS-220) sells for $299.



Greystone Peripherals Inc.
130-A Knowles Dr.
Los Gatos, CA 95030
(408) 866-4739
▶ **CIRCLE 592**

▼ MULTIMEDIA PRESENTATION CREATION MADE EASIER

Users can create interactive multimedia presentations in a free-form environment using the SST Windows-based software. SST supports all popular graphics, animation, sound, and digital-video formats. Context-sensitive help screens are available throughout the presentation creation process. All objects can be given motion, and text can scroll or move in any direction. Also, fonts and colors can be altered on the fly. Minimum system requirements include a 386SX-based PC, 2 Mbytes of RAM, a VGA display, Windows 3.1, and a mouse. The $149 price tag includes a user's guide and handbook, a tutorial, clip media, and sample slide carousels.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(612) 531-0603
▶ **CIRCLE 593**

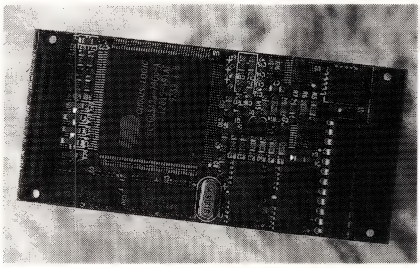
▼ 5.25-IN. DRIVES HOLD 3 AND 4 GBYTES

The DSP5400 and DSP5300 5.25-in. hard-disk drives represent the highest-capacity drives in that form factor, claims their developer, Digital Equipment Corp. The 5400 is a 4.0-Gbyte drive, while the 5300 holds 3.0 Gbytes. The SCSI-based drives, built with an embedded servo technology, incorporate banded recording and a multi-segmented cache buffer—1 Mbyte on the 5400 and 512 kbytes on the 5300. To ensure data integrity, the drives include 264-bit Reed-Solomon error-correction codes (ECCs) and end-to-end error-detection code (EDC). Both drives feature an average latency of 5.6 ms and an average seek time of 11.5 ms, which come from a 5400-rpm disk speed. The MTBF is rated at 500,000 hours. Available now, the DSP5400 sells for $3150, while the DSP5300 costs $2735, both in evaluation quantities.

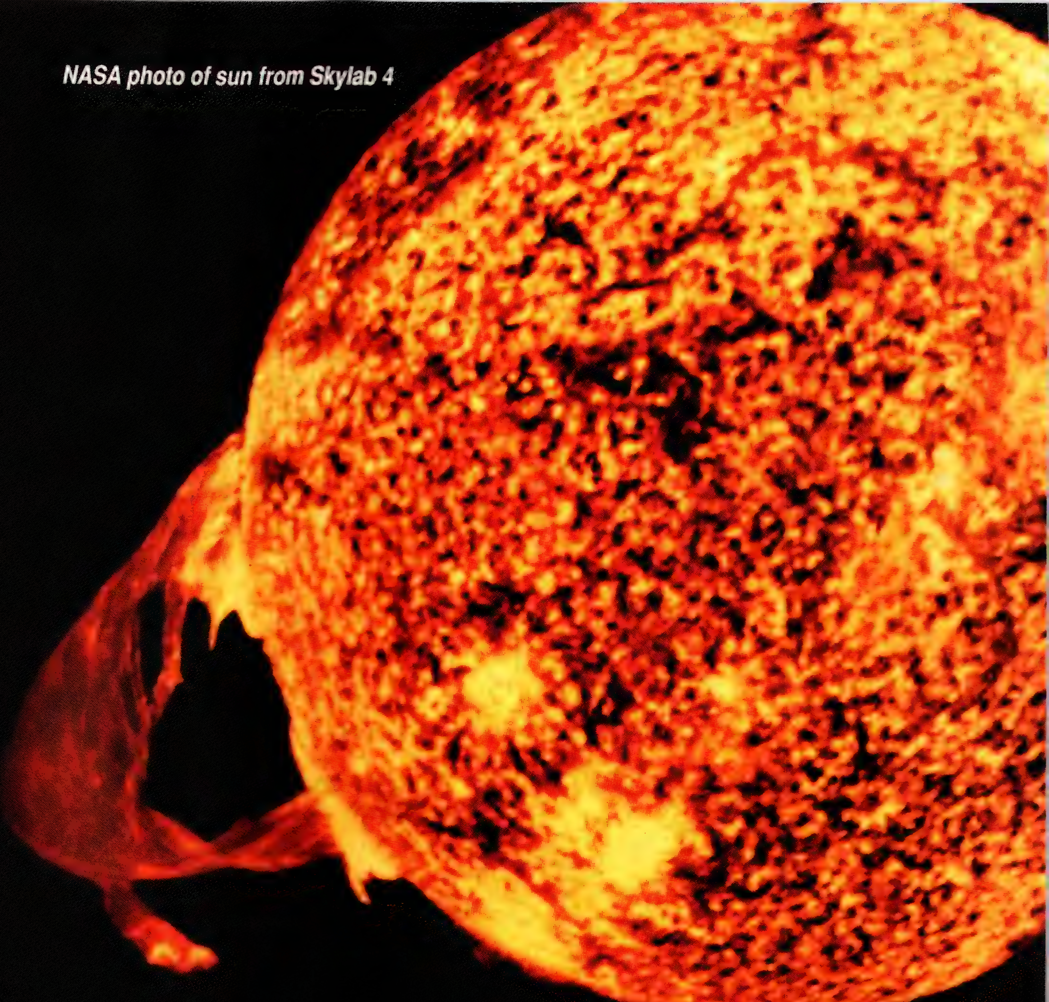
Digital Equipment Corp.
334 South St.
Shrewsbury, MA 01545
(508) 841-3111
▶ **CIRCLE 594**

▼ MODULE ADDS SVGA CAPABILITIES

IndustryPack mezzanine bus boards are small modules that connect to larger baseboards to supply special customization. One such board is the IP-SVGA, which adds Super VGA (SVGA) capabilities. It's compatible with Microware's Rave and X-Windows and Gespac's G-Windows, popular graphical user interfaces for industrial automation. Designed around a Cirrus Logic CL-GD5422 SVGA controller, the module supports 512 kbytes of VRAM and comes with all requisite filters and cable drivers. The mezzanine card supplies a direct connection between the host CPU and the video memory. The IP-SVGA, bundled with a Super VGA cable, sells for $395 and is immediately available.



GreenSpring Computers Inc.
1204 O'Brien Dr.
Menlo Park, CA 94025
(415) 327-1200
▶ **CIRCLE 595**



NASA photo of sun from Skylab 4

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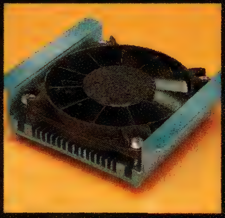

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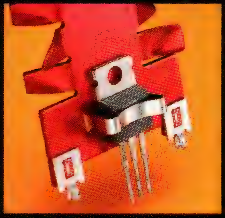

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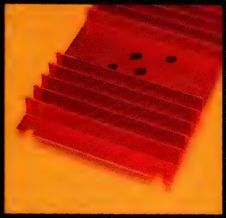
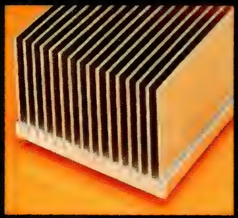


The higher the power, the more we can help.



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▼ SBUS BOARDS ACCELERATE 3D GRAPHICS

A series of Sbus boards, the GLengine-24XP and 48XP, increase the performance of the Sparc-based PX/Iris GL 3D library. Using the boards, 3D applications can be ported from a Silicon Graphics system to a Sun platform without compromising speed or quality. The boards supply true-color 24-bit graphics, a 4-bit overlay, and double buffering in a dual-slot Sbus format for any Sparcstation. The 24XP delivers 100,000 3D Gouraud shaded polygons/s and supports monitor resolutions up to 1152 by 900 pixels. The 48XP increases the resolution to 1408 by 1120 pixels. The GLengines can also be used to accelerate X-Windows and other Sun applications. Available now, prices start at $5495.

Du Pont Pixel Systems
2010 N. First St., Suite 403
San Jose, CA 95131
(408) 436-3455
▶ CIRCLE 596

▼ DSP BOARD PERFORMS FFTs

High-performance fast-Fourier-transform (FFT) processing capability comes to PC-compatible computers using the CRP1M40 single-slot DSP board. The board, based on Sharp's LH9124/LH9320 chip set, can perform a 1-k-complex FFT in 82.0 µs at 40 MHz and has a 48-bit-wide complex data path. The board isn't limited to ISA bus speeds because the external I/O bus architecture can be customized. The board can hold either 16- or 64-kbyte SRAM modules for processing 16- or 64-kpoint continuous complex FFTs, respectively. Applications include radar, image processing, spectrum analysis, and multichannel speech processing. The 40-MHz board is priced at $17,750. A lower-cost 25-MHz version is also available.

Catalina Research Inc.
985 Space Center Dr., Suite 105
Colorado Springs, CO 80915
(719) 637-0880
▶ CIRCLE 597

▼ 600 DOT/IN. ENGINE PRINTS 17 PAGES/MIN.

High-performance and high-duty-cycle printing are available from the LBP-NX 600 laser-beam printer engine. The 17-page/min. engine, with its 600-dot/in. resolution, is suited for network printing and on-demand publishing. The engine can be combined with the EP-N toner cartridge (which also holds the drum, whose particles are about half the size of conventional toners). The cartridge boasts an 8000-page print life. Up to 1000 sheets can be handled by the engine in its twin paper cassettes. An optional envelope feeder holds up to 100 envelopes. A user-installable duplex module permits double-sided printing.

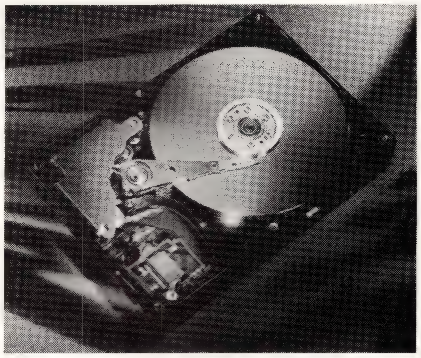
Canon USA Inc.
One Canon Plaza
Lake Success, NY 11042
(516) 488-6700
▶ CIRCLE 598

▼ OPTICAL DISK DRIVE IS PORTABLE

The Tahoe-130 magneto-optical disk drive uses a rechargeable battery pack to gain portability. The 3.5-in.-disk drive weighs 1.8 lbs. and measures 1.4 by 4.5 by 8 in. Each removable cartridge holds 128 Mbytes of data. The drive offers a 28-ms seek time and a rotational speed of 3600 rpm. The battery pack supplies 3.5 hours of typical use. Another feature of the drive is that it extends the battery life of the portable PC's batteries by eliminating the need to access the resident hard-disk drive. The rewritable drive connects to a SCSI interface or a parallel port. The Macintosh version of the Tahoe-130 sells for $999, while the PC model costs $1199. An extra battery and travel case sell for $199.

Pinnacle Micro Inc.
19 Technology
Irvine, CA 92718
(800) 553-7070 or
(714) 727-3300
▶ CIRCLE 599

▼ LOW-POWER DISK DRIVE STORES 1.08 GBYTES



Today's leading-edge servers, workstations, and disk arrays demand high performance from their attached hard-disk drives. One drive that's up to the task is the 3.5-in., 1.08-Gbyte 1080 drive. The 1080 represents a 20% reduction in parts from the previous generation and consumes just 6 W in idle mode. Other enhancements include a faster throughput due to a rotational-reordering scheme and a 5400-rpm spindle speed. The drive is also available with fast and wide SCSI interfaces to increase data transfer and is electrically compatible with the upcoming SCSI-3 standard. Moreover, the 1080 contains a 32-MHz microprocessor and a read-channel chip that can transfer 48 Mbits/s. The 1080 drive costs $995. A lower-capacity version is also available.

Quantum Corp.
500 McCarthy Blvd.
Milpitas, CA 95035
(408) 894-4000
▶ CIRCLE 600

▼ 15-IN. DISPLAY FEATURES POWER-DOWN MODES

The ViewSonic 15 color monitor has been upgraded to include some advanced power-management features. The "green" display conforms to the VESA low-power standard, meaning that it powers down in three stages by directly responding to the host system's video output signals. The time required to enable each stage is user programmable. The first stage (standby) reduces the power consumption to less than 80% of full-on. Power restoration is almost immediate. The suspend state draws less than 30 W. It takes about 4 s to return from this state. The final stage is off, where the display pulls in under 5 W. Recovery time is equal to that of an initial startup. The 15-in. flat square monitor offers a 0.27-mm dot pitch and a maximum non-interlaced resolution of 1280 by 1024 pixels. The ViewSonic 15 display sells for $599.

ViewSonic Inc.
20480 Business Pkwy.
Walnut, CA 91789
(800) 888-8583 or
(909) 869-7976
▶ CIRCLE 601

SINGLE CHIP PERFORMS PHYSICAL-LAYER FUNCTIONS FOR FIBRE CHANNEL, ESCON, SSA, AND ATM DATA LINKS.

TRANSCEIVER CHIP SERVES FOUR SERIAL INTERFACES

MILT LEONARD

By using smaller cables and connectors, high-speed serial links for portable PCs and multimedia desktops are nudging aside parallel interfaces that traditionally interconnect computers and peripherals. This trend is evident in development efforts that promise to complete several serial-interface standards this year.

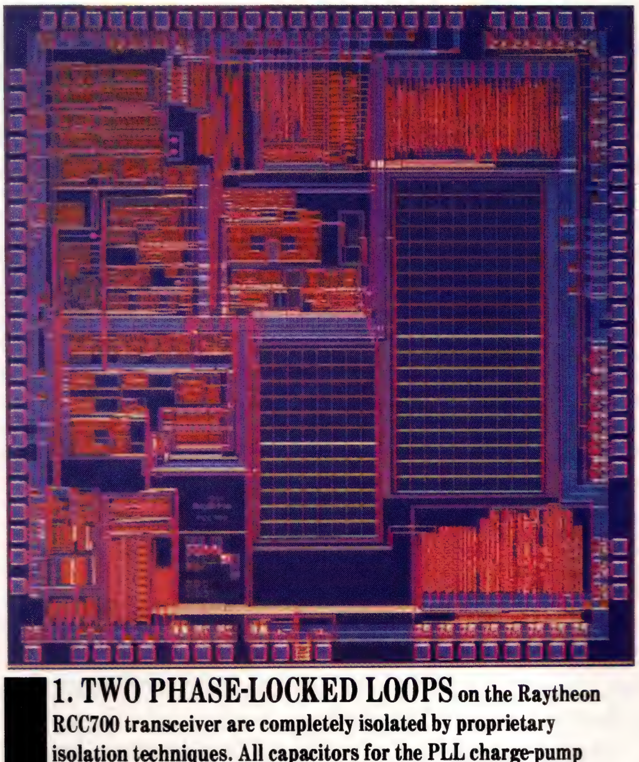
Of these standards, Fibre Channel is currently attracting the most attention because of its relatively high speed, low implementation cost, and application flexibility. Using either copper or optical-fiber cabling, its speed can be scaled up from 133 Mbaud to 1 Gbaud without software revisions.

A critical function in a Fibre Channel link is the transceiver. This circuit performs encoding/decoding, serialization, and multiplexing operations for the physical layer of a communications system. Early solutions from IC suppliers have included a bipolar two-chip transceiver/receiver from Cypress Semiconductor, a single-chip CMOS transceiver from NCR, and a two-chip gallium-arsenide (GaAs) transmitter/receiver plus a CMOS encoder/decoder from Triquint Semiconductor.

However, according to Raytheon Co., all of these solutions leave something to be desired. In general, present solutions are either too large, use too much power, are too costly, have limited performance, or require the use of external components to perform encoding and decoding.

Addressing these problems, the Semiconductor Div. of Raytheon has come up with the RCC700 CMOS transceiver *(Fig. 1)*. The RCC700 integrates all required transceiver functions in a single chip that consumes less power than bipolar and GaAs designs. Moreover, with data rates of 194.40, 200, and 265.625 Mbaud, the chip is not only compliant with the Fibre Channel, ESCON (IBM's 200-Mbits/s Enterprise System Connection standard for interconnecting IBM computers), and SSA (Serial Storage Architecture for interconnecting peripherals such as disk drives) standards, it also can be used as the physical transport for a 194.4-Mbaud asynchronous-transfer-mode (ATM) LAN.

The Fibre Channel standard is expected to be adopted by the American National Standards Institute (ANSI) this year. The standard defines data transfers between workstations, mainframes, and peripherals. Presently speci-

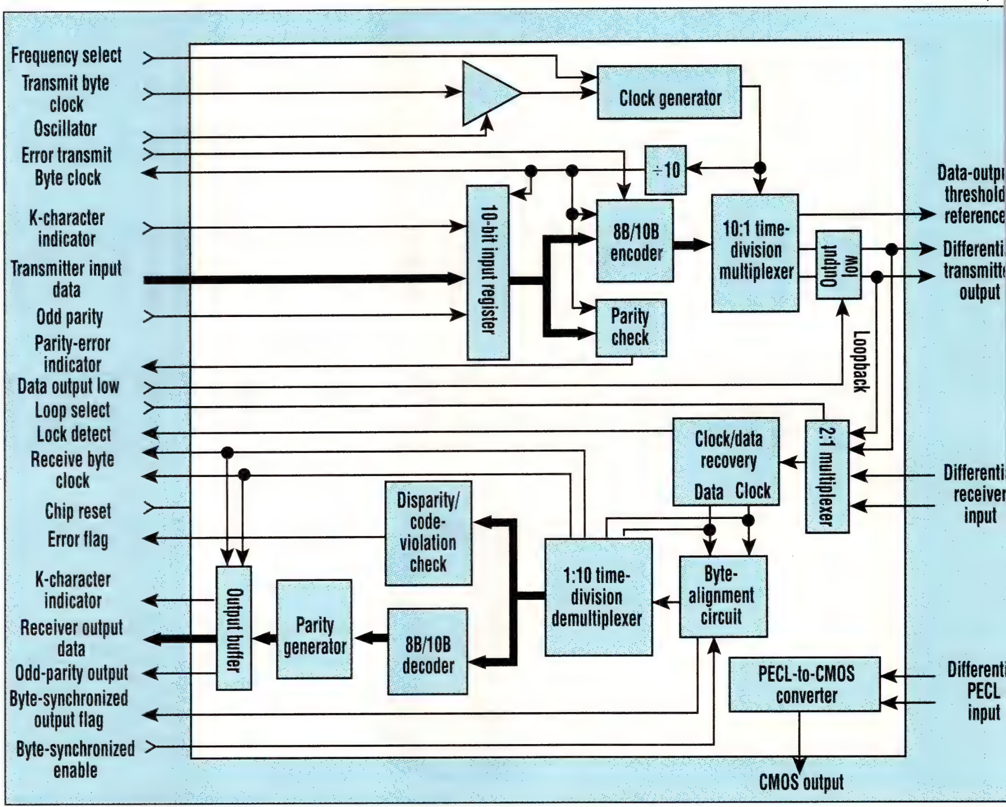


1. TWO PHASE-LOCKED LOOPS on the Raytheon RCC700 transceiver are completely isolated by proprietary isolation techniques. All capacitors for the PLL charge-pump circuitry are integrated on the chip (dark areas). Therefore, no external components are required.

fied data rates are 132.81, 265.265, 531.25, and 1062.5 Mbaud. Fibre Channel operates over a distance range of 0.5 to 10 km with optical-fiber cable, and up to 100 m for coaxial cable.

The Fibre Channel provides a common serial interface for other peripheral standards, such as HiPPI (High-Performance Parallel Interface), IPI (Intelligent Peripheral Interface), and SCSI (Small Computer Serial Interface). Fibre Channel is also the standard of choice for serial SCSI (SCSI-3). In addition, Fibre Channel defines a high-speed interface for transporting LAN data across network layers.

The RCC700 architecture is partitioned into transmitter and receiver sections *(Fig. 2)*. The transmitter portion accepts TTL-compatible, 8-bit parallel data, encodes the data with an 8B/10B coding algorithm, and serializes the encoded data with a 10:1 time-division multiplexer. Raytheon uses 8B/10B coding for its dc line-balancing characteristics, which are superior to 4B/5B code. The coding algorithm also enhances data integrity and limits the data run length (number of consecutive 1s or 0s) to optimize the receive function. Serial data exits the transmitter as a differential pseudo-ECL (PECL) signal to a fiber-optic transceiver module (for a fiber link), or to a driver/receiver (for a copper-cable link).



2. THE TRANSMITTER SECTION of the RCC700 transceiver accepts TTL/CMOS-compatible parallel data from a controller IC. It then encodes the data using the 10B/8B code, synthesizes the high-speed clock, and serializes the data into a differential PECL-compatible output. The receiver section performs the reverse operations as well as clock and data recovery.

The transmitter includes a phase-locked-loop (PLL) clock generator that multiplies an input frequency of 19.4, 20.0, or 26.56 MHz by a factor of 10. The input frequency can come from either an external crystal oscillator or an external protocol chip. There are also inputs for a K-character and a parity bit. The K-character input, which is asserted to turn data bytes into control bytes, is used for initialization, frame-alignment, and link-control functions. Parity is calculated on the data bits and compared to the received parity bit. If there's a difference, a parity-error flag is set.

To protect the transmitter diode in a fiber-optic module, the transceiver's data-output-low pin can be asserted to force the output to a low state. An error-transmit input enables the transmitter to send out error bytes for test and diagnostics. These bytes have alternate running disparities (1001111011 or 0110000100) to balance the line.

THE RECEIVER

PECL-compatible serial data from a fiber-optic or copper module enters the receiver section, which recovers the clock and data, performs byte alignment if necessary, deserializes the data, decodes 10-bit words, and outputs a TTL-compatible, 8-bit data byte plus a parity bit. The data is time-demultiplexed into 10 parallel bits and decoded into 8-bit data bytes by an 10B/8B decoder. Running disparities and coding are checked during decoding. Any violation sets the error flag.

The receiver section of the RCC700 includes byte-synchronization circuitry to determine the byte boundaries of the incoming serial data. A lock-detect function alerts the protocol layer if the incoming data and the voltage-controlled oscillator (VCO) aren't locked. A byte-sync signal indicates to the protocol layer that byte synchronization has been achieved. For testing purposes, a loopback feature can route transmitted data directly to the receiver section while the incoming serial data is disabled.

The RCC700 provides the physical interface for several serial data links. For Fibre Channel, the transceiver is used with a protocol chip and a driver/receiver module for either copper or fiber-optic cable. For ESCON and ATM systems, the transceiver is used with an ESCON/ATM protocol chip and a fiber-optic transceiver module. For SSA, the transceiver is used with a protocol chip to drive a twisted-pair cable.

The 200-Mbaud data rate for ESCON and SSA is significantly higher than existing parallel-link standards. ESCON operates over distances of up to 10 km when employed with a single-mode laser and up to 3 km with a multimode LED. SSA operates over distances up to 10 m.

The SSA standard provides dual porting for simultaneous read and write memory-disk operations. Dedicated inbound and outbound cables can each carry data at 20 Mbytes, equivalent to a serial data rate of 200 Mbaud, including overhead for 8B/10B encoding and decoding.

The RCC700 can also be used in ATM applications running at a line rate of 194.4 Mbaud, the equivalent of a 155-Mbit/s data rate with 8B/10B encoding/decoding overhead included. ATM is a fast cell-switching technology that uses labels for multiplexing and switching as opposed to positional multiplexing and switching in synchronous time-division-multiplexed systems.

ATM has two physical-interface standards at 155 Mbits/s. One standard addresses a Sonet-based scrambling technique for which the RCC700 doesn't apply. The other requires 8B/10B encoding, and can be implemented using the RCC700. Both shielded twisted-pair cabling and fiber cabling can be used for data transport. In either cabling case, a driver/receiver is needed to couple the signal to the transport.

As currently defined, ATM cells consist of 48 data bytes and five overhead bytes. The control bytes include a header for synchronization and error checking. The RCC700 operates with two external chips in the ATM data link. A segmentation and reassembly chip forms the cells from data on the host system bus, and reassembles data coming from the serial interface. A cell delineation chip adds the necessary overhead for checking errors, defining destinations, etc. The RCC700 receives data, control, and timing signals from this chip.

The RCC700 can also be used for bus extension in point-to-point data links and to eliminate timing-skew problems associated with running parallel cables in serial video communications.

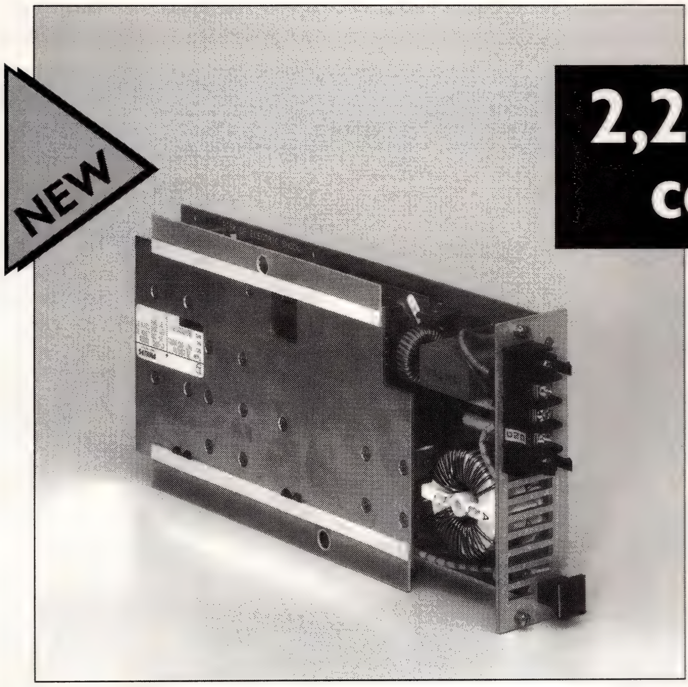
Operating from a single 5-V power supply, the RCC700 is fabricated on a submicron CMOS process and dissipates 600 mW at a 200-Mbit/s data rate. No external components are required. Package options include a 68-pin PLCC and a 64-pin PQFP measuring 14 by 14 by 2 mm.☐

PRICE AND AVAILABILITY

In quantities of 10,000 units, the RCC700 Fibre Channel transceiver chip is available now for $33.20 each in the 64-pin PQFP and $32.10 each in the 68-pin PLCC.

Raytheon Co., 350 Ellis St., Mountain View, CA 94039-7016; Jack Guedj, (415) 968-9211. **CIRCLE 511**

HOW VALUABLE?	CIRCLE
HIGHLY	530
MODERATELY	531
SLIGHTLY	532



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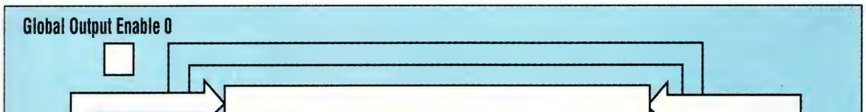
TWO COMPLEX PLD FAMILIES LET DESIGNERS RUN SYSTEMS AT 135 MHZ OR TRIM CHIP COUNT WITH 14-KGATE PROGRAMMABLE LOGIC ARRAYS.

DAVE BURSKY

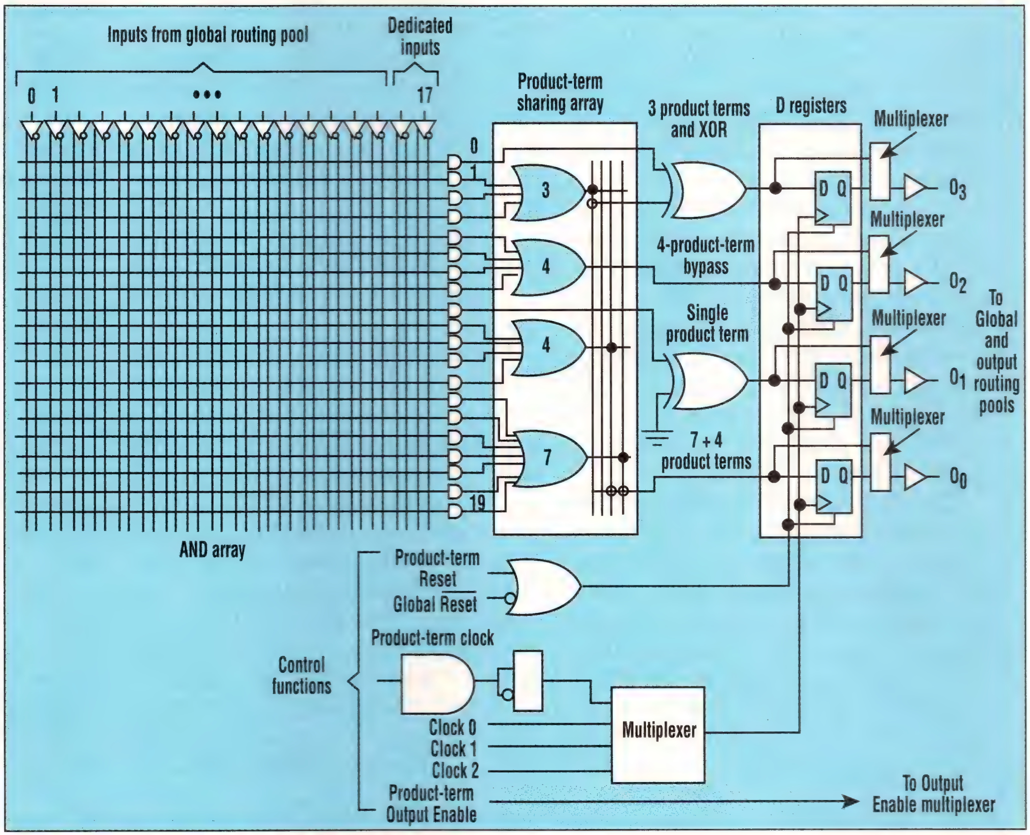
Increasing complexity in programmable logic devices presents designers with two key challenges: How to maintain the short propagation delays found in the low-complexity devices while achieving the high functionality possible with gate-array alternatives. To address both of these areas, two enhanced families of high-density programmable logic were developed by Lattice Semiconductor. Both families will use the company's electrically-erasable programmable logic devices (E^2PLDs). Each will come in Lattice's standard programmable LSI (pLSI) and in its unique in-system programmable LSI (ispLSI) form.

The first of the two families, the 2000 series, offers the shortest propagation delays for complex PLDs. The other family, the 3000 series, focuses on gate density, I/O count, and enhanced testability through the use of an IEEE 1149.1-compatible boundary-scan test port. Each family will initially have three density options. Both will join the company's original pLSI and ispLSI 1000 families of E^2CMOS high-density PLDs.

The 2000 family, with operating frequencies up to 135 MHz and pin-to-pin logic delays of as little as 7.5 ns, suits many of the applications that currently



1. THE OVERALL ARCHITECTURE of the just-released 2000 and 3000 series of enhanced programmable logic circuits is similar to that of the original 1000 series. At the heart of the circuits, developed by Lattice Semiconductor, is a global routing pool (GRP). Surrounding the GRP are the macrocells, which are in turn are surrounded by the output routing pools and the I/O pads.



2. EACH GLOBAL LOGIC BLOCK (GLB) used in the pLSI/ispLSI 2000 series offers a similar level of functionality as the GLBs in Lattice's original pLSI 1000 series. The blocks, which provide 18 inputs, 20 product terms, and 4 register outputs, are well suited for control applications. The more complex macrocell used in the 3000 series packs close to double the functionality and more readily handles data-path type functions.

employ high-speed but low-density PLDs. This series also widens the logic density and I/O count beyond the levels available in the earlier 1000 family. In part, the high speed was achieved by using the company's 0.65-μm, UltraMOS V E^2CMOS process. Additional speed gains were the result of architectural streamlining.

The family's three density options—the 2032, 2064 and 2096—contain the equivalent of 1000, 2000, and 4000 PLD gates, respectively. Those gates are divided among 8, 16, and 24 generic logic blocks (GLBs), respectively, on each of the three chips. Each GLB possesses 20 product-term inputs and provides four registered or combinatorial outputs. It allows the designer to configure each of the four GLB flip-flops as a JK-, T-, or D-type element, and gives the designer multiple clocks for synchronous or asynchronous applications. Inputs and I/Os total 34 for the 2032, 68 for the 2064, and 102 for the 2096. Package options include PLCC, plastic quad flat pack (PQFP) and thin quad flat pack (TQFP), with pin counts ranging from 44 to 128 leads.

Taking the high road in terms of logic density, I/O counts, and features, the 3000 family will initially offer three densities ranging from 8000 to 14,000 PLD-type gates—the 3192, 3256, and 3320. The pLSI and ispLSI versions will offer top clock speeds and minimal propagation delays that span from 110 MHz/10 ns for the 3192 to 80 MHz/15 ns for the 3320. These chips provide 24, 32, and 40 programmable GLBs, respectively, with inputs and I/O pins totalling 96 for the 3192, 128 for the 3256, and 160 for the 3320.

The 3000-family GLBs are more complex than those in the 2000 series—each 3000-series GLB has 24 inputs from the global routing pool and 8 register outputs. That gives the series 3000 almost twice the complexity of the 2000 series, considerably improving the flexibility and ability to implement more-complex functions in the GLB. The programmable circuits will be available in 128-, 160-, and 208-lead PQFPs.

The ispLSI version in all three families makes it possible for them to be programmed using only a standard 5-V power supply and a five-wire serial interface. In-system programmability addresses many of the manufacturing concerns voiced by companies using fine-pitch, high-pincount programmable devices on surface-mount pc boards. By eliminating separate programming steps and socketing operations, ispLSI chips minimize concerns about bent device leads and out-of-specification lead coplanarity due to handling.

Providing short-delay programmable logic to support high-performance system designs has been the exclusive domain of low-density but fast PLDs. High-speed address decoding and minimal-delay bus-controller functions must typically operate at twice the processor clock frequency. Even the fastest 20- and 24-pin PLDs have been hard-pressed to keep up with the performance requirements of the Pentium, Alpha, and other RISC and CISC CPUs.

The Pentium's 66-MHz clock rate dictates that the support logic operate at speeds of at least 132 MHz. Thanks to Lattice's UltraMOS V process, the 44-pin, 8-GLB pLSI and ispLSI 2032, which operate at 135 MHz, are now the first high-density PLDs to exceed this threshold (the 132-MHz minimum frequency). And because the 2032 integrates the equivalent of 4 to 6 low-density PLDs like PALs into a single package, designers can cut power consumption and board space by up to 6:1.

The 2000 family architecture is similar to that of the earlier 1000 family. It consists of a central global routing pool (GRP) surrounded by the programmable GLBs *(Fig. 1)*. The GRP adds a fixed delay of less than 2 ns between any two points on the device. That limits signal skew and possible logic hazards while enhancing performance.

A second level of programmable interconnect, the output routing pool (ORP), provides programmable routing between the outputs of the GLB and the I/O cells. The ORP gives designers more freedom in selecting the pin assignments—other high-density PLD architectures often associate one fixed I/O pin with each logic-cell output.

The GLB found in all three of Lattice's high-density PLD families shares a common set of programmable features: an input AND array that feeds a programmable product-term sharing array (PTSA), which in turn feeds some exclusive-OR gates that deliver the signals to the registers or directly to the output-routing matrix *(Fig. 2)*. For example, the 2000-family GLB programmable logic array takes 18 inputs from the GRP and generates combinatorial AND-OR functions. The outputs of the OR gates are routed through the PTSA, in which common functions can be efficiently shared and incorporated into multiple GLB output functions. The integral XOR gates make the GLB particularly efficient in handling arithmetic and comparator functions.

For very-high-speed functions, the PTSA can be bypassed to give the fastest input-to-output path. The registers in the GLB can be independently programmed for either JK-, T- or D- operation. In addition, multiple clock options, including product-term clocking, make synchronous circuit implementations easier.

Sticking to its role as a fast, cost-conscious family of devices, Lattice took a "lean and mean" approach with the 2000-family architecture. For example, unlike the original 1000- and the new 3000-family architectures, the 2000 devices don't incorporate dedicated I/O registers at the device pins. That's because most of the applications expected for the 2000 family will consist primarily of control logic rather than data-path functions. Control functions usually don't require signal latching at the device pins. Thus, Lattice's designers eliminated the infrequently used feature, reducing the chip size, chip cost, and ultimately the selling price.

In the 3000 family, Lattice's inclusion of twin GLBs lets the circuits implement data-path-oriented structures (each twin contains twice the programmable logic of the GLB used in the 1000 and 2000 families). Consequently, the new 3000 family GLB is more silicon-efficient, allowing higher logic densities, while supporting up to 24-bit functions. With the twin GLB, the 3000 family devices provide from 96 (the pLSI/ispLSI 3192) to 480 (3320) registers in one device.

The 3000 family also is enhanced significantly by the integration of

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dedicated boundary-scan logic into the I/O structure. The 3000-family devices include IEEE Standard 1149.1-compliant JTAG (Joint Test Advisory Group) circuitry, which allows the scan data pattern to be shifted in or out. As part of the JTAG port, each device includes a test-access-port (TAP) controller and associated I/O scan registers. All mandatory 1149.1 public instructions are supported, including Bypass, Sample/Preload and EXtest. The boundary-scan feature enables complex-pc-board and systems designs to exhaustively test overall logic functionality to ensure the highest quality and reliability levels.

The isp programming interface and boundary-scan TAP in the 3000 family use the same set of four pins, selected by an isp/boundary-scan mode-select pin. Clock, Serial Data In, Serial Data Out, and Mode control pins are present in both interfaces. By combining in-system programming and boundary scan, design and manufacturing engineers will be able to define new test methodologies, for more thorough testing and higher quality.

The capacity, testability, and performance of the 3000 series devices make them ideal for implementing complex system functions such as DMA, LAN, and memory subsystem controllers, as well as high-performance glue-logic integration. In contrast to the 2000 family, which aims at control functions, the 3000 family will be used to implement significant data-path functions, including adders and multipliers. As a result, the 3000-series chips include the dedicated I/O registers that were originally introduced in the pLSI 1000 family.

Design-tool support for the new families includes PC-based support from Lattice's pDS design tool. The pDS provides a complete Windows-based design tool, including Boolean entry and design editing along with automatic logic routing. Lattice currently provides support for popular third-party design environments on the PC and Sun platforms, such as pDS+ Viewlogic, pDS+ ABEL and pDS+ LOG/iC design fitters. Viewlogic's Viewsim timing simulation and Logic Modeling system-level simulation models are also available. Support for Cadence, Mentor Graphics and Synopsys design tools is also planned.☐

PRICE AND AVAILABILITY

The pLSI and ispLSI 2032 are available now in 44-pin PLCC packages and sell for $10 and $12 each, respectively, in 1000-unit lots. The pLSI and ispLSI 3256 are available now in 167-lead pin-grid-array packages and are priced at $175 and $210 each, respectively. The remaining devices in the pLSI and ispLSI 2000 and 3000 families will be released during 1994.

Lattice Semiconductor Corp., 5555 Northeast Moore Ct., Hillsboro, OR 97124; Stan Kopec, (503) 681-0118. **CIRCLE 513**

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MODERATELY	545
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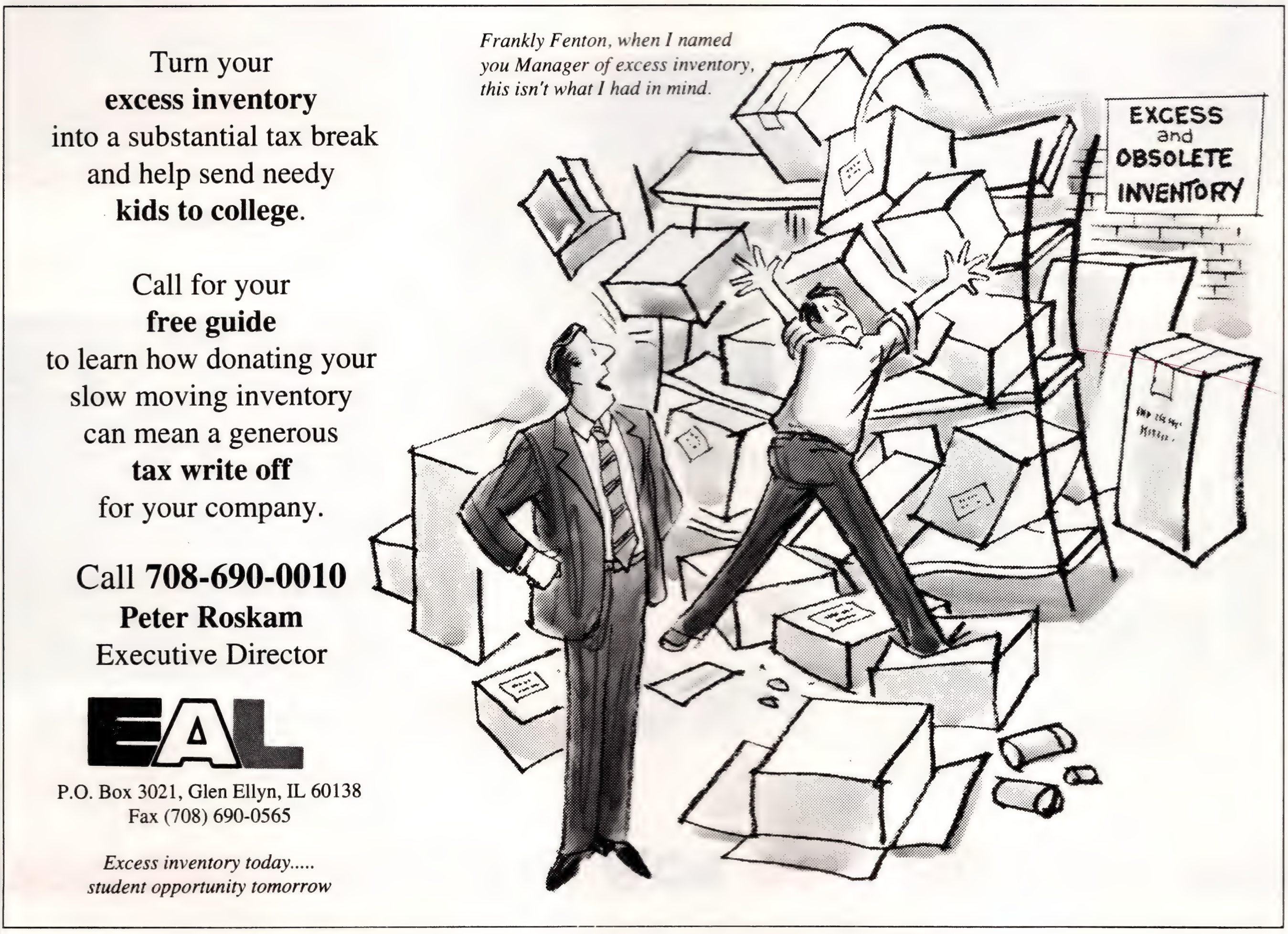
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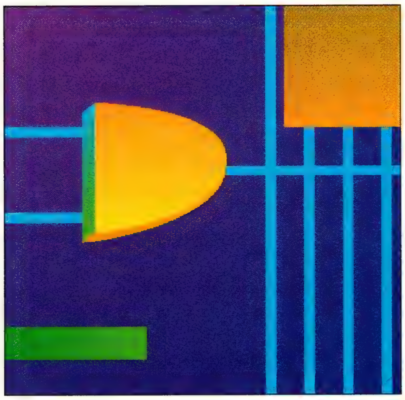

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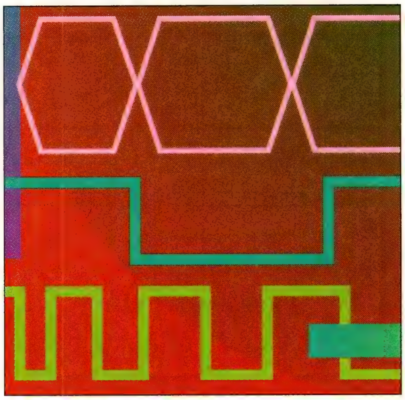

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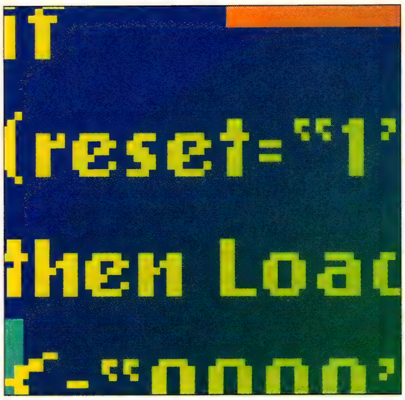

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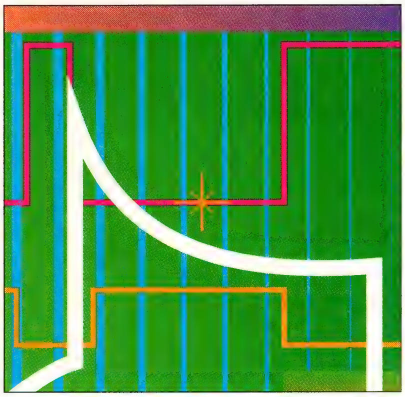

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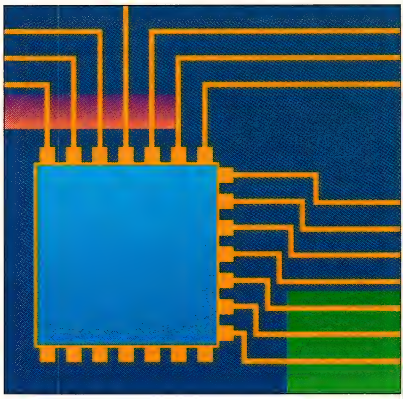

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CIRCLE 259 FOR U.S. RESPONSE CIRCLE 260 FOR RESPONSE OUTSIDE THE U.S.

PRODUCTS NEWSLETTER

LOW-POWER DRAMS EXTEND SYSTEM LIFE

With the ability to operate at 3.3-V, a family of low-power 4-Mbit dynamic RAMs developed by Hitachi America Ltd.'s Semiconductor and IC Div., Brisbane, Calif., trims memory operating power to the lowest levels to date. The DRAMs also include self-refresh circuitry, thus permitting the chips to maintain data even when the rest of the system is powered down. The refresh logic generates a refresh cycle about every 200 μs—about 13 times slower than the active-mode refresh rate, reducing the power drain and extending portable-system battery life. On standby, the DRAMs typically consume just 50 μA. There are nibble, byte, and word-wide versions of the DRAMs, and available speed grades include devices with access times as short as 60 ns. The HM51W4400B/BL is a 1 Mword-by-4-bit unit; the W4800A/AL is a 512-k-by-8 memory; the W4260A/AL is organized as 256-k-by-16, employs a 512-cycle/8 ms refresh, and has two CAS inputs; the W4160A/AL has the same by-16 organization but uses a 1024-cycle/16 ms refresh and has dual write-enable lines; the W4170A/AL is similar to the W4160A/AL but has dual CAS lines. All DRAMs come in low-profile (1.2-mm thick) thin SOP-II packages, reducing board-space requirements. Prices range are $20 to $23 each in 1000-unit lots. Production quantities are immediately available. Contact Farhad Tabrizi, (415) 244-7235. *DB* **CIRCLE 612**

CONVERT 5 V TO 3 V EASILY ON A BOARD

Aimed at converting 5-V rails on a pc board to a 3-V rail wherever a chip needs it, the 2-V power Zener, which Semtech Corp., Newbury Park, Calif., calls the EZ Dropper, has been upgraded. The new models are aimed at lower currents. These unique devices, announced late in 1992 (ELECTRONIC DESIGN, Dec. 17, 1992, p. 37) are not truly Zener diodes from a "black-box" point of view, but they look like Zeners (they are actually V_{be} multipliers). Connected between a 5-V rail and a 3-V load, the devices require no large capacitor on their inputs and outputs, unlike a low-drop-out linear regulator; neither does any of their current pass to ground rather than to the load. The original EZ5Z3 series, specified for currents from 100 mA to 1 A, were upgraded to provide a current range from 10 mA to 1 A. The new lower current EZ5Z3L series, available in a TO-92 package as well as the original SOT223 and TO-220 packages, allow users to place them directly at the load reducing pc-trace line drops. They are specified for operation at currents from 5 mA to 250 mA. All models are available with adjustable output versions as well as 3- and 3.3-V versions. Pricing starts at $1.86 each in lots of 100. Call Art Fury, (805) 498-2111 ext. 230. *FG* **CIRCLE 613**

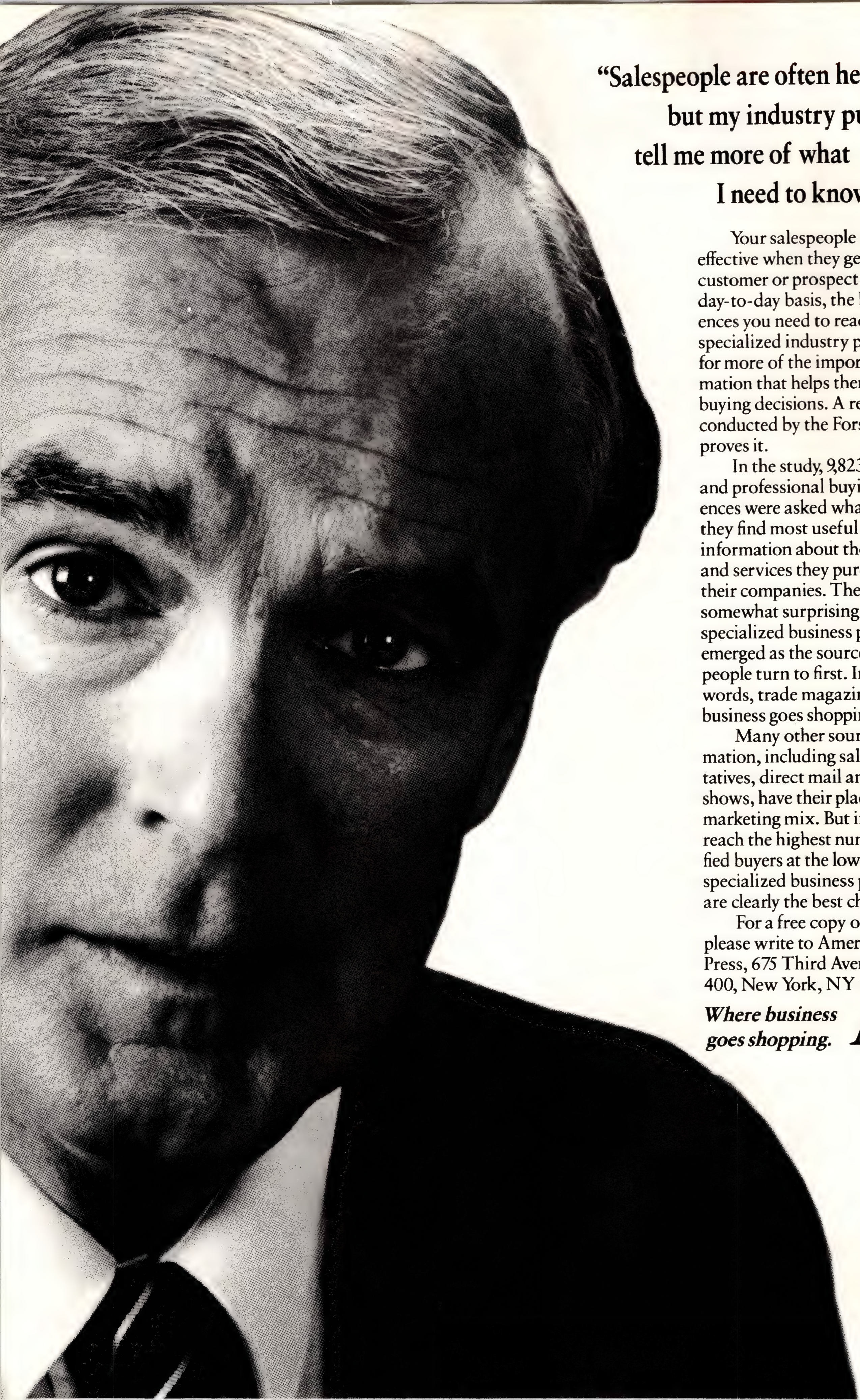
AUDIO CHIP SETS OFFER MOTHERBOARD SOLUTION

Low power consumption and a high functionality make the Jazz and Jazz16 audio chip sets versatile performers for computer OEMs that want to integrate multimedia audio across their entire product line. The Jazz chip set from Media Vision Inc., Fremont, Calif., includes the MVD1208 8-bit audio controller, the MVA408 8-bit codec, and the MVA514 mixer. Together they offer a complete 8-bit motherboard solution for less than $18 in large quantities. The Jazz16 delivers a 16-bit solution and includes the MVD1216 audio controller, the MVA416 codec and the MVA514 mixer. Both chip sets offer functionality equivalent to a complete add-in sound board. Both are Sound Blaster compatible and include a MIDI transmit and receive port, a joystick interface, and other value-added features. The Jazz16 chip set costs $21.50 in 25,000-unit purchases, and the Jazz chip set costs $17.50. Samples are available now. *JS* **CIRCLE 614**

SDA TOOL GETS MORE TRACEABILITY

Aiming to give design engineers robust tools to handle complex system design problems, i-Logix has enhanced its system design automation (SDA) tool, Statemate 5.0, to support advanced requirements traceability, chart-level instantiation, and an interface to Cadre Technology Inc.'s Teamwork CASE environment. In enabling the modeling of multiple instances or copies of a common element within the Statement environment, i-Logix, of Burlington, Mass., embarks on support for object-oriented modeling. New to version 5.0 is the ability to link requirements directly to the design. The tool enables engineers to move easily from textual requirements to graphical specifications. Contact the company for pricing: (617) 272-8090; fax -8035. *SVT* **CIRCLE 615**

Edited by Clifford Meth



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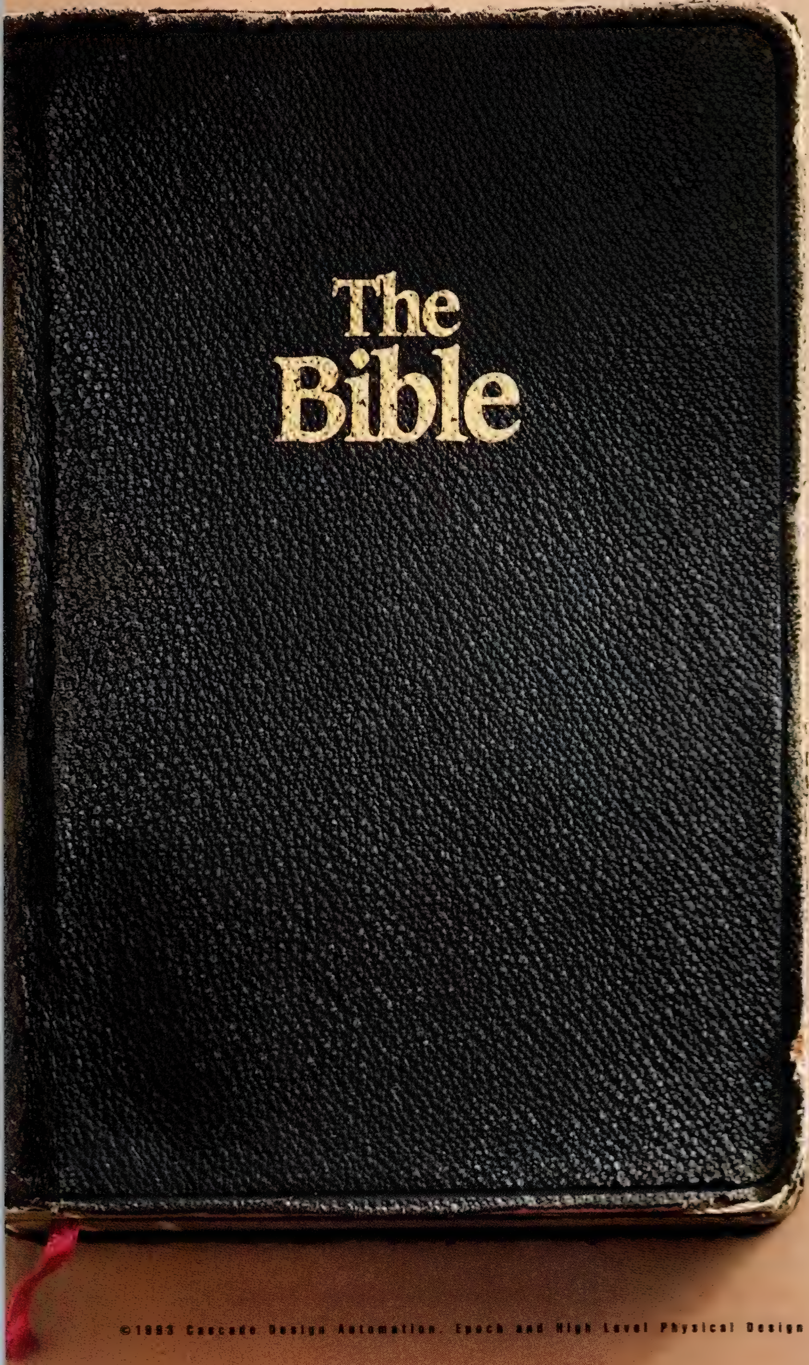
In the study, 9,823 business and professional buying influences were asked what sources they find most useful in providing information about the products and services they purchase for their companies. The results were somewhat surprising. Overall, specialized business publications emerged as the source business people turn to first. In other words, trade magazines are where business goes shopping.

Many other sources of information, including sales representatives, direct mail and trade shows, have their place in the total marketing mix. But if you want to reach the highest number of qualified buyers at the lowest cost, specialized business publications are clearly the best choice.

For a free copy of the study, please write to American Business Press, 675 Third Avenue, Suite 400, New York, NY 10017.

Where business goes shopping. **ABP**

The Next Time They Swear Their Physical Design Tools Can Perform Miracles, Make Them Swear On This.



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CIRCLE 102 FOR U.S. RESPONSE CIRCLE 103 FOR RESPONSE OUTSIDE THE U.S.

DAT DRIVES PACK UP TO 16 GBYTES/TAPE, AUTOLOADER HOLDS 64 GBYTES

DAVE BURSKY

Although not the first 4-mm DAT drives to incorporate the DDS2 double-density compression standard, the Model 3300DX and 3400DX digital audio tape (DAT) drives and the LD4-3400DX autoloader subsystem from WangDAT give users 4 to 64 Gbytes of on-line storage in a 3.5-in. or 5.25-in. full-height package. The drives incorporate a new cassette transport mechanism that reduces wear, improves head-to-tape contact, and extends the mean time between failures to over 180,000 hours (with a 30% duty cycle).

The 3.5-in. full-height 3300DX DAT drive can store 4 to 8 Gbytes on a 120- meter 4-mm cassette through use of the DDS or DDS2 algorithms. Average search time on the cassette is about 40 seconds (120 seconds worst case), while data can be transferred at up to 366 kbytes/s. The model 3400DX also incorporates the enhanced DDS2-DC compression format that squeezes up to 16 Gbytes onto the same 120-m tape and ups the data transfer speed to 732 kbytes/s. Either drive can have a SCSI-1 or SCSI-2 interface (via a factory installed module) and both include a 1-Mbyte buffer memory to maximize burst transfers over the SCSI bus.

To improve the drive's reliability, WangDAT designers revamped the entire tape path to prevent tape damage. Roller guides were added to reduce tape friction, and the entire tape path, except for the read/write head contact is all on the non-oxide surface of the tape, thus minimizing oxide wear. Designed to handle the thin tape, the mechanism includes a brake lock to prevent tape from spilling if power is inadvertently removed from the drive; as a result, tape breakage and tangles are minimized. Furthermore, to prevent dust from damaging the tape, a motor-controlled cover keeps the cassette path sealed.

In many cases the drives end up in systems with limited air flow and that could cause overheating. With that in mind, designers added the equivalent of a fan inside the DAT drive by attaching a bladed plastic cap to the rotating read-write head. The "fan" helps pull air through the drive to keep the temperature more constant across the drive. The read/write head also received a redesign to make sure the tape stays in contact with the head.

For storage requirements that exceed a single tape's storage capacity, the LD4-3400DX autoloader subsystem employs a four-cassette magazine that yields 32 to 64 Gbytes of total capacity. Extensively tested, the autoloader mechanism has an MTBF of over 210,000 hours—even better than the DAT drive itself. The subsystem consists of the 3400DX DAT drive and an enclosure that holds a four-cassette magazine and also provides a single-cassette load path directly into the drive.

The magazine that holds the cassettes is not a "stack" scheme with cassettes arranged one on top of another. Rather, the cassettes are spring- loaded and set in two layers, with two cassettes on each layer. The four cassettes can be cycled between the autoloader and the magazine to provide either a sequential or a random-access capability to the stored data.

A SCSI driver program to control the media changer mechanism is all that's needed to move the cassettes and manage the data. Such programs are available from several suppliers—TapeWare, Dantz Retrospect, Cheyenne (LD4) ArcServe, and others. A write-lock switch on the magazine overrides the individual cassette write-lock tabs, thus providing uniform control over when the cassettes can be written to.

The base drives require 5 V at 1 A and 12 V at 0.85 A, maximum, for a worst-case power of about 15 W (less than 7 W typical). About 40% more power is required for the autoloader version. The 3.5-in. drives weigh in at about 2 lbs. apiece, while the autochanger comes in at about 5 lbs.

In lots of 500, the autoloader subsystem sells for less than $2000 apiece, while a distribution-oriented version goes for about $5000 in single-unit lots. The base drives—the 3300DX and 3400DX—sell for $1465 and $1660, respectively, in single-unit lots, and for less than $1000 apiece in lots of 500. Samples are available now.

WangDAT, 140 Technology Dr., Irvine, CA 92718; Amar Samra, (714) 753-8900. **CIRCLE 620**

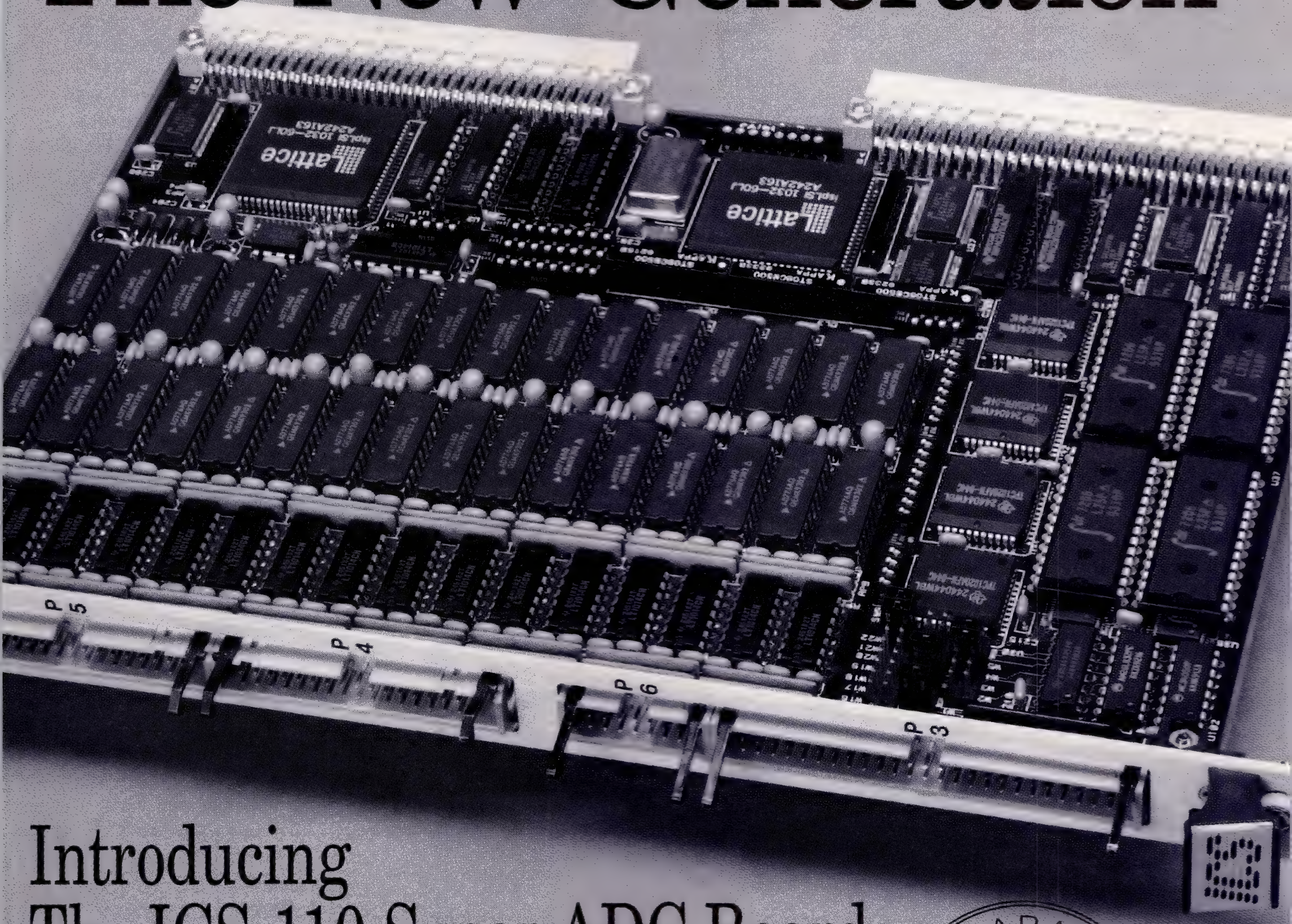
UPGRADE X TERMINAL TO WORKSTATION

The SparcClassic X computer is an X terminal that features a low-cost plug-and-play upgrade to a workstation. The system delivers from 29,000 to 102,600 Xstones, depending on configuration. It's based on a 50-MHz microSparc processor and comes with 4 or 8 Mbytes of RAM (expandable to 96 Mbytes), a local window manager, and installation and administration software. Either color or gray-scale configurations are available. Users can run DOS-based applications, such as Windows 3.1, using a DOS emulator. To upgrade the X terminal to a workstation, users simply add more memory, a hard-disk drive, and a Solar is object-code license. This turns the system into a complete SparcClassic workstation. The system is also compliant with the EPA's Energy Star program for reduced power consumption.

The SparcClassic X system, with 4 Mbytes of RAM and a 15-in. color display, sells for $2545. The minimum cost to upgrade that X terminal to a fully-configured SparcClassic workstation is $2550. RN

Sun Microsystems Inc., 2550 Garcia Ave., Mountain View, CA 94043; (415) 960-1300. **CIRCLE 621**

The New Generation



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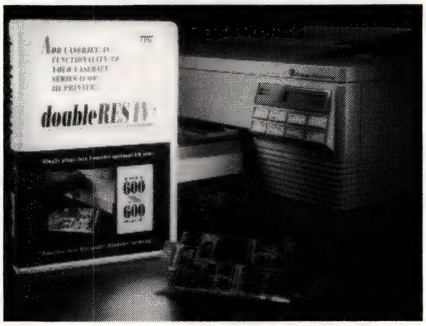

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Tandem Computers Inc., 19191 Vallco Pkwy., LOC 4-40, Cupertino, CA 95014; (408) 285-6000. **CIRCLE 623**

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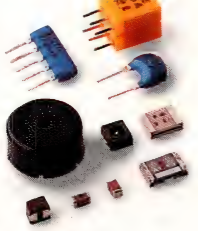

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HIGHLY-INTEGRATED ALPHA CPUS TARGET DESKTOP AND EMBEDDED SYSTEMS

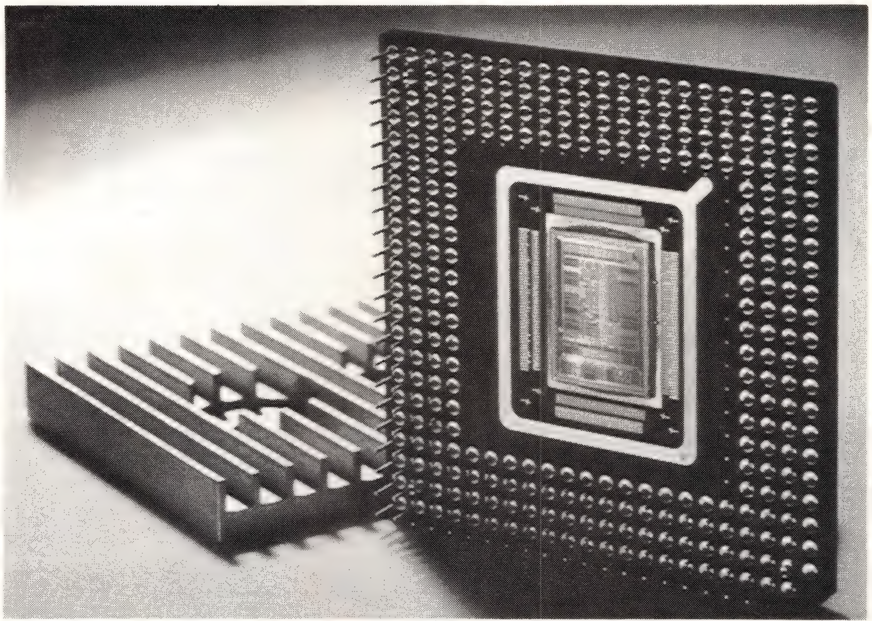
DAVE BURSKY

The first microprocessor of any type to integrate the high-performance peripheral component interconnect (PCI) bus right into the CPU, the 21066 and 21068 Alpha RISC processors from Digital Equipment provide highly-integrated solutions for desktop computers and embedded control systems. By integrating the PCI bus as well as other features—a memory controller for main-memory, graphics memory, and cache memory; a programmable phase-locked-loop clock multiplier, and a graphics accelerator—the two new chips ease the design of Alpha-based systems.

The 21066 is targeted at computer systems that run Microsoft's Windows NT operating system—the CPU can internally run at 166 MHz and at that speed delivers about 70 integer SPECmarks and about 105 floating-point SPECmarks. The 21068 is basically the same chip, but is internally clocked at just 66 MHz. That trims the active power of the CPU from about 20 W to just 8 W, and makes the chip more attractive for embedded-control applications. The slower clock, however, reduces the 21068's performance to 30 integer and 50 floating-point SPECmarks—still very respectable numbers and better than most other high-end controllers.

To save chip area and reduce cost, designers reduced the system data path interface to 64 bits rather than use the 128-bit-wide bus employed by the original 21064 Alpha chip. This allows the new CPUs to go into a less-expensive, 237-lead pin-grid array package as opposed to the 431-lead PGA used by the first Alpha.

The core section "borrowed" from the original chip includes the CPU, the 8-kbyte instruction and 8-kbyte data caches, and the high-performance floating-point unit. To reduce system complexity, DEC designers first added the PCI-bus interface to the core. The PCI bus provides a high-speed interface with multiplexed address and data lines that



can take advantage of a broad range of Ethernet, SCSI, and other support chips, including an Intel-designed 16-bit ISA-bus-interface bridge.

Next, a memory controller was added to the core. The controller provides the multiplexed DRAM address signals, as well as the row- and column-strobe signals, to control four banks of 64-bit-wide memory. The memory-control block also directly controls a VRAM-based frame-buffer memory that is used by an integrated graphics accelerator. The buffer can be implemented by replacing one of the banks of DRAMs with a VRAM-based SIMM. The VRAM-based accelerator can deliver a throughput of 30 million Winmarks and operates on 1-, 2-, 4-, 8-, 16-, or 32-plane frame buffers. Although for moderate-performance systems this graphics buffer obviates the need for a separate graphics chip, DEC is developing an accelerator chip to provide even higher graphics performance.

Part of the memory controller block also generates the direct address and control signals needed to control up to 2 Mbytes of secondary cache memory and the external tag RAM. To simplify CPU and system clocking needs, a phase-locked loop frequency multiplier was also added. This section accepts a moderate-frequency external clock signal and multiplies it by any integer value between 2 and 9, with a maximum output for now of 166 MHz in the case of the 21066, and 66 MHz for the 21068.

The Alpha chips are designed for operation in either 3.3-V or mixed 3.3-/5-V systems. On a typical motherboard, the main part of the system can be powered by a 5-V supply and can directly interface to the I/O pins of the 21066 or 21068. To power the processors, a separate regulator that reduces the 5-V supply to the 3.3-V level is all that must be added.

To support computer system designs, DEC created a fully packed evaluation motherboard and a design package that contains schematics, bills of materials, and so forth. In contrast to the first Alpha chip, which was characterized as performance at any price, the 21066 and 21068 deliver performance at competitive prices. The CPUs sell for $385 and $221 each, respectively, in lots of 5000 units. Samples are immediately available.

Digital Equipment Corp., 77 Reed Road, HL02-2/M09, Hudson, MA 01749; Art Swift, (508) 568-5149.

CIRCLE 624

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S4 - THE PACKAGE

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CIRCLE 253 FOR U.S. RESPONSE CIRCLE 254 FOR RESPONSE OUTSIDE THE U.S.

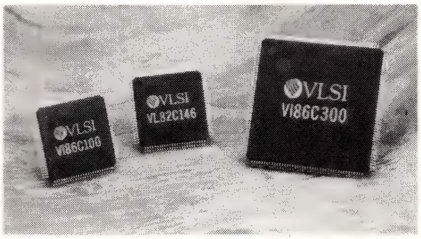
TWO-CHIP SET BASED ON 386SL CORE SIMPLIFIES PALMTOP SYSTEM DESIGNS

DAVE BURSKY

Bringing the level of system integration for 80386 CPUs to a new high, the joint design efforts from Intel and VLSI Technology have created the first 386-based chip set for personal digital assistants. The two-chip set, dubbed Polar, will initially be used by Compaq Computer Corp., Houston, Texas, in a new family of "mobile companion" systems it expects to introduce in 1994. On two chips, the design teams merged the processor with all the control and support logic and optimized it for ROM execute-in-place operating systems and embedded applications. The chip set includes the 386SL CPU and cache, a display controller, a digitizer input, an audio output, serial and parallel I/O ports, and a multiplexed local expansion bus (the ML bus).

Using its standard cell expertise, VLSI Technology took the Intel-developed 386SL processor core and other support functions and created two chips, the VL86C300 and the 86C100. The VL86C300 contains the static 386SL CPU, 2 kbytes of write-through cache and the cache controller, a two-word-deep posted-write buffer, a DRAM controller that supports up to 16 Mbytes of main memory, a direct memory interface for SRAMs or non-volatile memories that addresses up to 56 Mbytes of static memory (SRAM, EPROM, ROM, flash, etc.), and the 16-bit ML expansion bus. It will come in a 176-lead thin, plastic, quad-sided flat package (TQFP).

Also on the VL86C300 is a graphics controller with acceleration logic that can handle LCD panels as large as 640 by 480 pixels with up to 16 gray levels and a separate ink plane. To keep the system-level parts count low, the main system memory also doubles as a dumb, linear frame buffer, eliminating the need for a separate video memory for the graphics controller. The integrated processor/controller chip also has seven general-purpose I/O pins. Two of these I/O pins be employed as programmable chip-select lines to control external memory or I/O mapped devices.



The supporting VL86C100 comes in a 100-lead TQFP and adds many of the I/O support functions—a keyboard interface, two 82C59 interrupt controllers, an 82C54 counter-timer, two serial ports (one is a 16C550-compatible UART while the other is compatible with the Hewlett-Packard infrared serial link scheme that VLSI licensed from Hewlett-Packard), an audio input/output capability, and a digitizer-tablet serial-input port with 32-bit FIFO buffer. The Hewlett-Packard infrared port is compatible with the IR port Hewlett-Packard uses on its 95LX, 100LX, and Omnibook pocket-sized computers.

The audio I/O block on the companion chip includes a three-channel 8-bit a-d converter and a 10-bit successive-approximation a-d converter. The d-a converter used in the 10-bit successive-approximation a-d converter also doubles as the audio output d-a converter. The three-channel 8-bit a-d converter can be used to monitor battery voltage, temperature, or charge or discharge rate, or still other items. The higher-resolution 10-bit a-d converter is better suited to voice-store-and-forward applications as well as audio playback.

The ML-bus serves as the chip set's main expansion bus, providing a connection to the outside through PCMCIA interfaces supplied by yet another chip, the VL82C146, which was released earlier this year. The optional PCMCIA chip supports full hot insertion without requiring additional logic and provides power-management features including socket-power control and 3.3/5-V suspend operations.

Both chips are designed for operation from either 5- or 3.3-V power supplies at clock frequencies of 20, 25, or 33 MHz. At the maximum clock frequency, the power consumption for the chip set is about 600 mW. However, the static CMOS logic used on the chips permits the clock to be reduced to zero when the system is idling, thus dropping the CPU power drain to microwatts. The system management interrupt mode allows background software to manage the system power drain, turning off different subsections when they are not in use.

Although this first chip set is a "standard" product, the design is malleable because it was implemented with VLSI's functional-system-block standard-cell design tools and library. That would allow large customers (for a fee) to actually customize the chip set to their application by deleting some blocks, perhaps adding proprietary blocks or just modifying existing blocks.

A typical system configuration employing the Polar chip set would typically take the two-chip set and add several banks of DRAM, some flash memory or ROM/EPROM/SRAM, one or more PCMCIA controllers, a keyboard and/or an LCD panel with pen-input digitizer and some audio and serial I/O lines. The 86C300's address space can address 16 Mbytes of DRAM, 64 Mbytes of non-volatile memory, and up to 64 Mbytes mappable for use by PCMCIA cards.

The operating system tuned for the Polar chip set will be developed jointly by Microsoft Corp. (Redmond, Wash.), Compaq, Intel, and VLSI. The two-chip set sells for $50/set in lots of 10,000. Samples will be available later this year; production quantities in the second quarter of 1994.

VLSI Technology Inc., 8375 South River Pkwy., Tempe, AZ 85284; Chris Vance, (602) 752-6345.

CIRCLE 625

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"Colon cancer is a disease that afflicts more than 150,000 Americans each year and eventually kills over half. Yet, any doctor will tell you that with early detection, the survival rate could be raised to as much as 90%.

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Research was conducted from July 1989 to July 1990 in 4 markets in 10,000 households, at the equivalent of $21.3 million worth of air time, the average amount of donated time behind Advertising Council spots.

After six months of being exposed to one commercial, awareness of colon cancer among adults 40 and over rose from 11% to 29%.

After a year, awareness reached 40%.

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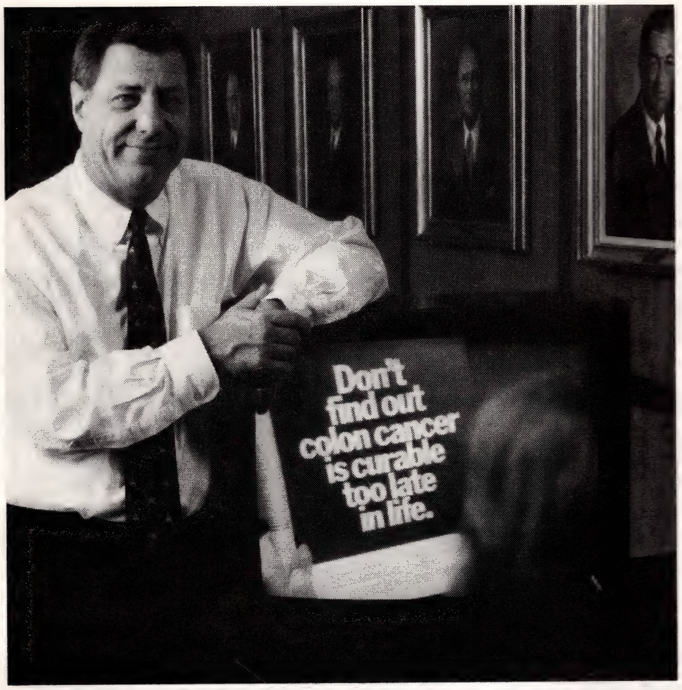
Oh, there's one more thing. If you're over 40, ask your doctor about colon cancer."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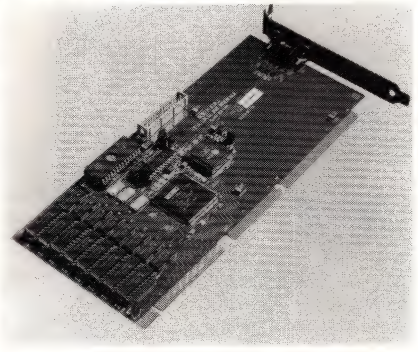
This advertisement was prepared by Calet, Hirsch & Ferrell, Inc., New York, New York: Photo: Fred Weber.

PLUG-IN GUI ACCELERATOR CARD INTERFACES TO THE VL-BUS

To attest to the fact that the VL-Bus local bus is gaining in popularity, NCR Corp. designed its 77C32BLT graphical user interface accelerator (GUI) with a VL-Bus interface after dropping an ISA-compatible part. The low-cost chip works with DRAM and features a 32-bit architecture that boosts pixel rates to 110 MHz on a 1280- by 1024-pixel non-interlaced display.

At the heart of the accelerator is a BitBLT engine which draws and moves pixel blocks at all color depths, including 24-bit true color. The engine also performs alignment, masking, color expansion, pattern fetch, and embedded clipping without any intervention from the host CPU. Special algorithms for drawing and moving text accelerate the use of spreadsheets and word processors.

The company claims that the accelerator is the first to support the Display Power Management Signaling (DPMS) proposal from the Video Electronics Standards Association (VESA). The proposal introduces low-power modes to facilitate the design of "green" PCs. Complete integration of the VL-Bus interface eliminates external glue logic and removes the delays associated with external decode and interface circuitry. As a result, there's plenty of free space on the board for OEMs to increase functionality. Instead of using an ISA bus interface for the video BIOS, a utility bus supplies direct interfacing of the BIOS and RAMDAC.



Housed in a 208-pin PQFP, the 77C32BLT is priced at $28 in large quantities. A 32-bit PCI-based version of the chip, the 77C832, will be available in October, possibly followed by a 64-bit PCI accelerator.

***NCR Microelectronics Inc.**, 1635 Aeroplaza Dr., Colorado Springs, CO 80916; (800) 334-5454 or (719) 596-5795.* CIRCLE 626

■ *RICHARD NASS*

SCSI-TO-VL-BUS CHIP SPEEDS DATA TRANSFERS

Simplifying the integration of SCSI disk drives into VESA VL-Bus based systems, the 92C108 interface chip performs 32-bit address and data transfers every three local CPU clock cycles. The controller is a high-performance VL Bus master and supports simultaneous overlapping data transfers from the local bus to the on-chip buffer and from the on-chip buffer to the SCSI DMA bus.

The chip has two DMA channels each supported by a 32-byte FIFO buffer. The VL-bus side of the chip can operate at bus speeds of up to 50 MHz, while the SCSI DMA channels each operate at up to 4 Mbytes/s. Each channel has a self-preempt capability and supports a VL-bus write-back capability. The DMA control interface provides 16-bit burst-mode data transfers with DMA read/write capabilities. A memory-buffer interface lets the chip address up to 128 kbytes of SRAM buffer space. Data loaded to the buffer can be transferred at maximum rates of 40 Mbytes/s.

Address, data and control signals are compatible with microcontrollers such as the 80196, thus permitting some local intelligence and access to a local EPROM for program control. The chip's internal buffer interface includes an internal priority resolver that allows the chip's four ports (data transfer channel, bus master interface controller, SCSI port, and local processor and host computer) to access the buffer RAM. The buffer interface also provides an internal block counter that keeps track of the data block's availability for transfer and prevents data overrun and underrun conditions.

In quantities of 1000 the 208-lead PQFP-housed chip sells for $62 each. DB

OPTi Inc., 2525 Walsh Ave., Santa Clara, CA 95051; Waqas Khan, (408) 980-8178. CIRCLE 627

4-MBIT SRAM MODULES EMULATE MONOLITHICS

Substituting for the hard-to-get monolithic 4-Mbit static RAMs, the DPS512S8PLL SRAM module provides 512k 8-bit words in the same 600-mil-wide 32-pin DIP pinout used by monolithic memory ICs. The module contains four 128-kword-by-8-bit low-power SRAMs, a high-speed CMOS decoder, and decoupling capacitors—all mounted on a co-fired ceramic substrate with side-brazed leads. The rigid substrate eliminates the problems of pin breakage and circuit damage that often occurs when inserting or removing pc-board-based modules that feature soldered-on leads.

Operating from a 5-V power supply, the modules have versions with standby power levels of as little as 25 μW, typical. Speed grades range from 70 to 150 ns. A high-speed version—the DPS512S8AP—that accesses in as little as 25 ns, is also available. Housed in a 36-lead SOJ plastic package is another version of the 4-Mbit module that comes in speed grades from 20 to 55 ns. The package is 400-mils wide, 5.5-mm high, and comes with center power and ground leads.

Prices for the SRAM DIP modules, in lots of 1 to 100 units, are $117 to $124 each, depending on the access time of the memory. The 25-ns high-speed version costs $233 each in similar quantities. The SOJ version, the DPS512R8J4, costs $162 to $247 each for the 55- and 20-ns access-time units, respectively.

Dense-Pac Microsystems Inc., 7321 Lincoln Way, Garden Grove, CA 92641-1428; Al Kile, (714) 898-0007. CIRCLE 628

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Chart I	Actel	Actel	Xilinx	Altera
Device	A1240A	A1240A-2	XC4005A-5	EPM7256-20
Capacity[1]	15.3	15.3	15.4	14.7
Performance[2]	36.3 MHz	48.4 MHz	35.0 MHz	45.3 MHz
Price[3]	$68.80	$96.30	$138.70	$214.25

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Chart II	Actel	AMD
Device	A1225A	22V10Q-25
# Devices	1	12
Total Icc Power[4]	10 mA	660 mA
Total Price[5]	$42.50	$69.36

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1. Average number of PREP instances, approximately 4000 gates or 20 PALCE22V10s. 2. PREP Derived Data-average internal operating frequency, in MHz. 3. 100 piece PQFP price quoted by authorized distributor, August/September 1993. 4. Typical Icc per device multiplied by number of devices. 5. Based on 100 piece PLCC price quoted by authorized distributor, August/September 1993. ACT, PLICE, Designer, and the Actel logo are trademarks or registered trademarks of Actel Corporation. PREP is a trademark of the Programmable Electronics Performance Corporation. All other brand or product names are property of their respective holders.

CIRCLE 82 FOR U.S. RESPONSE CIRCLE 83 FOR RESPONSE OUTSIDE THE U.S.

MULTIMEDIA PROCESSOR HANDLES TELEPHONY

A fully programmable digital-signal processor specifically designed for real-time processing of multimedia software applications has been enhanced to handle concurrent audio and telephony. The DSP3207 is a redesigned version of the company's DSP3210, which was introduced in 1991 and has a 72-ns instruction cycle. The DSP3207 is intended to run with AT&T's VCOS operating system, which has also been enhanced for concurrent audio and telephony.

In addition to concurrent multimedia, the chip delivers enhancements such as improved power management. But its major architectural change is the repartitioning of I/O from core DSP functions. This allows system designers more opportunity to differentiate their products. The chip's power-down mode is significantly better than the DSP3210's and an even lower power mode as been added that virtually shuts down the chip when not in use.

The DSP3207 is sampling now and will go into volume distribution in the fourth quarter of 1993. Pricing is not available. JS

AT&T Microelectronics, Dept. AL-500404200, 55 Union Blvd., Allentown, PA 18103; (800) 372-2447 ext. 885; fax (215) 778-4106.

CIRCLE 629

SPEEDY GAL PLDS ADD ZERO-POWER MODE

Taking aim at "Green" system designs, the 12- and 15-ns versions of the GAL 16V8 and 20V8 have added a zero-power mode that drops their standby power drain to less than 100 μA, maximum (50 μA, typical). The two CMOS PLD types also have an active current of 55 mA, maximum, and can operate up to 83.3 MHz. The electrically reprogrammable GALs can be 100% tested to ensure full functionality. The 20-lead GAL16V8Z-12Q and the 24-lead 20V8Z-12Q use input-transition-detection to control power-down operation—if there are no transitions on the chip inputs for a predefined time period, the chips enter their standby mode. Any activity on the inputs causes the GALs to switch back to their active mode. Other versions, the GAL16V8ZD-12Q and 20V8ZD-12Q employ a dedicated power-down pin to enter the standby mode, eliminating the timeout delay and permitting system designers to control all the circuits in a system with a global power-down signal. Prices are $2.20 to $4.25 each, depending on speed grade and package type (DIP or PLCC), in 1000-unit lots. DB

Lattice Semiconductor Corp., 5555 Northeast Moore Court, Hillsboro, OR 97124-6421; Steve Stark, (503) 681-0118. **CIRCLE 630**

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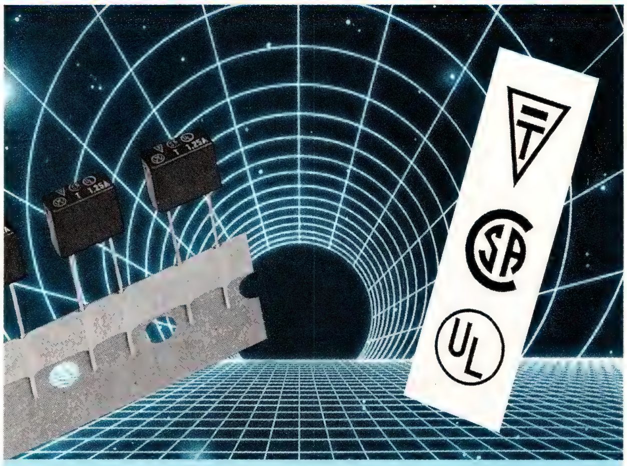
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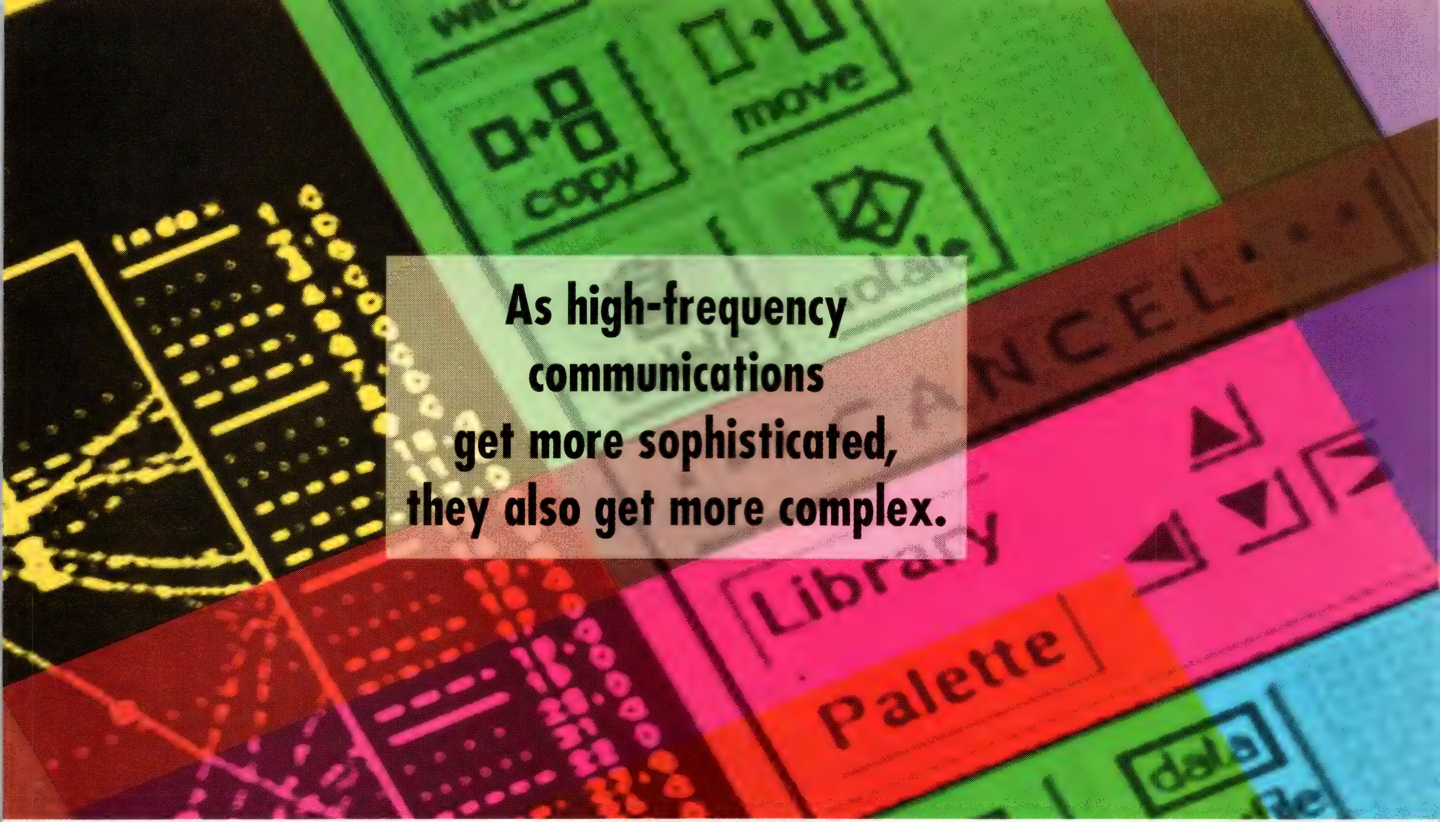

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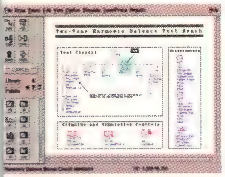

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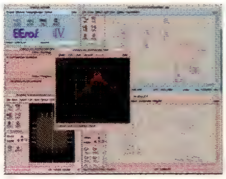

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SCSI 1 & 2

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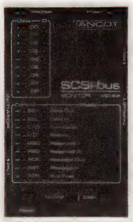
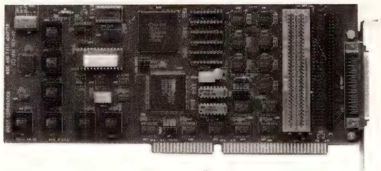
Target Emulator



Bus Monitor

Mutiplexer Switch



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CIRCLE 193 FOR U.S. RESPONSE

CIRCLE 194 FOR RESPONSE OUTSIDE THE U.S.

WINDOWS-BASED SOFTWARE ALLOWS GRAPHICAL TEST PROGRAMMING

HP VEE, a graphical programming language for design engineers and manufacturing test engineers, is now available in a Windows version. With HP VEE, engineers create test programs by using mouse clicks to connect icons into block diagrams.

High-level building blocks combined with features of a standard programming language reduce programming complexity and increase flexibility. Also, highly interactive test development capabilities like interactive edit/run, interactive visual debug, and instant changes eliminate the need to search through code to make changes.

HP VEE for Windows' visual user interface employs "soft" front panels to offer a picture of instrument settings. Users can sequence several tests, with branching based on the results of tests. Over 300 drivers for HP instruments are included, and a robust driver writer tool makes it easy to create custom drivers. The software supports Windows features like dynamic link libraries and dynamic data exchange, and gives users several ways to integrate code written in Basic, C, or other languages.

HP VEE for Windows runs on IBM-compatible 386 and 486 PCs with Windows 3.1 or later and DOS 5.0 or later.

HP VEE for Windows costs $995. Add-on analysis and manufacturing modules cost $595 each. A bundle with the base package and both modules goes for $1995. A run-only version costs $495.

***Hewlett-Packard Co.**, Direct Marketing Organization, P. O. Box 58059, MS51L-SJ, Santa Clara, CA 95051-8059; (800) 452-4844.* **CIRCLE 631**

■ *JOHN NOVELLINO*

TEST SOFTWARE SUPPORTS FULL AND PARTIAL SCAN

CyCheck is a flexible, high-performance test solution that supports a broad range of design-for-test (DFT) techniques, including full and partial scan. The software accommodates stuck-at, I_{DDQ}, and toggle fault models. Advanced features and algorithms allow users to maximize test coverage and eliminate time-to-market delays caused by testability. The solution includes testability analysis, a DFT rules checker, test synthesis, good and fault simulation, and automatic test-pattern generation. The testability analysis capability allows users to interactively explore various alternatives to improve design testability. The software accepts standard netlist and ASIC library formats and outputs standard vector and netlist formats. CyCheck initially runs on Sun workstations, but will be available for other platforms at a later date. JN

CheckLogic Systems Inc., 2290 N. First St., Suite 215, San Jose, CA 95131; (408) 955-9009. **CIRCLE 632**

FUNCTION GENERATOR DOES ARBITRARY WAVES

The HP 33120A 15-MHz function/arbitrary waveform generator uses direct digital synthesis techniques to supply stable, accurate output signals. The unit delivers clean, low-distortion sine waves, fast rise- and fall-time square waves, and linear triangle and ramp waveforms down to a 10-μHz resolution. Vertical resolution is 12 bits. In the arbitrary mode, the sampling rate is 40 Msamples/s and the waveform memory is 16 ksamples. Users can store up to four 16-ksample or eight 8-ksample waveforms. Internal modulation capabilities include am, fm, FSK, and burst modulation. Linear and log sweeps, with rates from 1 ms to 500 seconds, are built in. IEEE-488 and RS-232 interfaces are standard, and all functions are programmable. The HP 33120A costs $1695. JN

Hewlett-Packard Co., Direct Marketing Organization, P.O. Box 58059, MS51L-SJ, Santa Clara, CA 95051-8059; (800) 452-4844. **CIRCLE 633**

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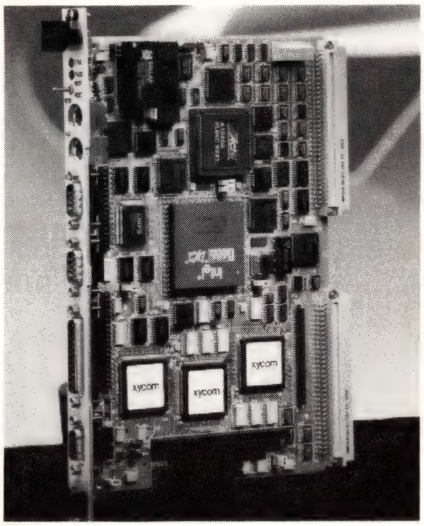
AT-COMPATIBLE SYSTEM FITS 6U VME FORM FACTOR



The XVME-674VME-based processor board from Xycom incorporates the functionality of a PC/AT computer, 32-bit VMEbus master and slave interfaces, and a PC/104 expansion connector on one 6U board. It comes with either a 33-MHz 486DX processor or a 66-MHz 486DX2 chip. There's also a socket for upgrading to a P24T CPU for Pentium performance. The board holds up to 32 Mbytes of dual-access DRAM and 1 Mbyte of video RAM. An on-board Super VGA controller supports resolutions up to 1024-by-768 pixels with 256 colors, and features a BitBlt engine for graphical user interfaces. The board is customized using the PC/104 expansion port for parallel and serial ports, memory, and Ethernet and SCSI functions. Pricing for the XVME-674 starts at $3950. RN

Xycom Inc., 750 North Maple Rd., Saline, MI 48176; (313) 429-4971. **CIRCLE 634**

SERIAL DATA PASSES AT T1 AND E1 RATES

Eight channels of serial data can be passed at T1 and E1 rates using the VCOM-54, a VME64-compatible communications controller. The board is built with two Motorola 25-MHz 68360 quad integrated communications controller (QUICC) multiprotocol engines. Each 32-bit processor, handling four channels, can be accessed through the VME P2 connector or an optional front-panel configuration. Front-panel access to serial ports is done using a mezzanine line-interface module that holds either four or eight ports. The VCOM-54 holds up to 4 Mbytes of parity-protected DRAM. The board is software compatible with Motorola's 68020 microprocessor. A software-application kit contains configuration utilities, serial-port drivers, and programming examples. Available now, the eight-channel board, with 4 Mbytes of memory, is priced at $3285 in quantities of 100. RN

SBE Inc., 4550 Norris Canyon Rd., San Ramon, CA 94583; (800) 925-2666 or (510) 355-2000. **CIRCLE 635**

ACCELERATOR BOOSTS HP WORKSTATIONS

The HP 9000747i and 742rt VME computers can become fully integrated 2D graphics workstations using the Maxim accelerator board. The board boosts performance by using a coprocessor architecture and 16 Mbytes of on-board dedicated memory for storing images, pixel maps, and fonts. The coprocessor manages such tasks as the manipulation of bit and pixel maps and fonts.

The single-slot 6U board's features include multiple screens and users, selectable screen resolutions ranging from 640 by 480 pixels to 1600 by 1280 pixels, and graphics speed up to 1.4 million vectors/s. Initially, the board will support HP-UX 9.0, followed by HP-RT. It can also run an accelerated version of X-Windows. RN

Megatek Corp., 9645 Scranton Rd., San Diego, CA 92121; (619) 455-5590. **CIRCLE 636**

MAC SYSTEM CREATES PROFESSIONAL VIDEO

High-quality NTSC or PAL video programs can be created directly from a Macintosh computer using the Media 100 digital video production system. The package lets users digitize, store, and edit analog audio and video using a picture-based interface. Then, the finished product can be recorded back onto a video tape.

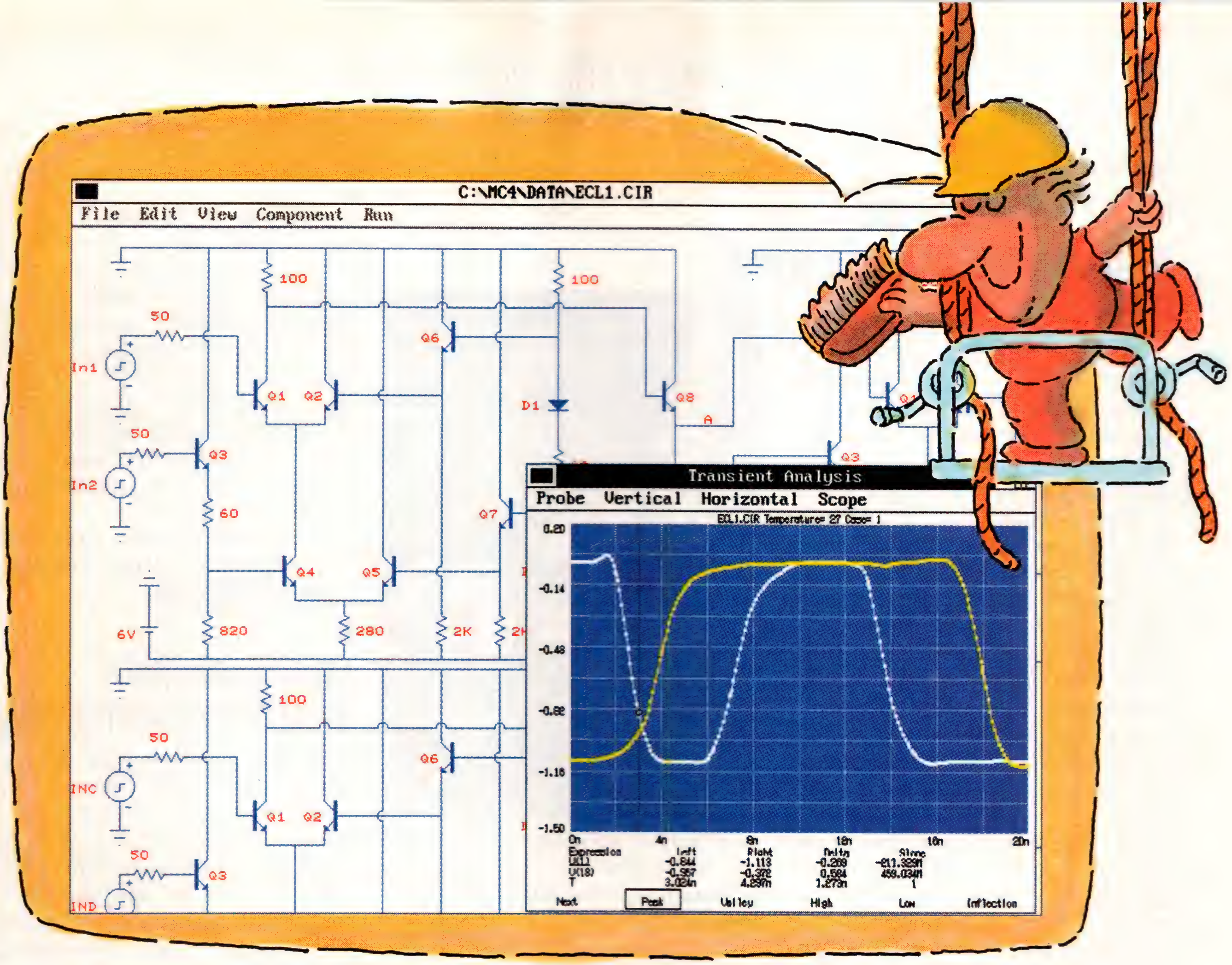
The Media 100 system consists of two NuBus boards and video-production software that's compatible with Apple's System 7 and QuickTime software. Minimum hardware requirements include a Macintosh Quadra with two available slots, 24 Mbytes of RAM, a SCSI hard-disk drive, a video monitor, and a video tape recorder. Available now, the Media 100 system sells for $11,995. RN

Data Translation Inc., 100 Locke Dr., Marlboro, MA 01752; (508) 460-1600. **CIRCLE 637**

PORTABLES CONNECT TO MILITARY COMPUTERS

Portable computers can communicate with military tactical systems and peripherals through the AT/NTDS parallel interface. The half-size board conforms to Mil-STD-1397B, and works in either NTDS types A (slow) or B (fast) modes. An NTDS emulator created with the interface can be taken into the field. The product's full-duplex, 32-bit I/O interface allows for parallel communications with independent I/O channels. Transfer rates between systems are 250,000 32-bit words/s in the fast mode, and 41,667 in the slow mode. The AT/NTDS interface sells for $2695. A military cable adapter is available for $750. RN

Sabtech Industries, 5411 E. La Palma Ave., Anaheim, CA 92807; (714) 693-3500. **CIRCLE 638**



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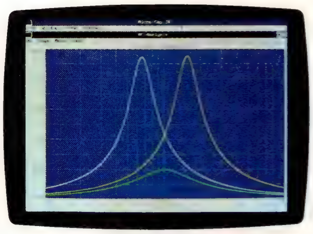
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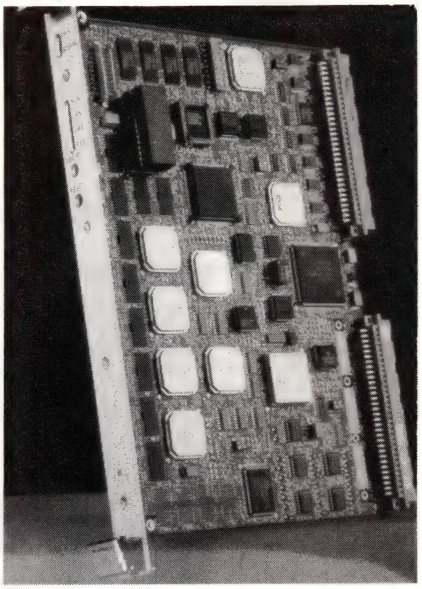
CIRCLE 226 FOR U.S. RESPONSE

CIRCLE 227 FOR RESPONSE OUTSIDE THE U.S.

88110-BASED SBCS ADD SECONDARY CACHE

The MVME197 family of high-end VME single-board computers from Motorola's Computer Group has two new members—the 197SP and the 197DP. The boards' high performance makes them suitable for such applications as telecommunications and simulation. The performance comes from the addition of secondary cache memory and, on the 197DP, dual processors. Both are based on the company's MC88110 symmetric superscaler RISC microprocessor. The boards serve as the CPU for the company's recently announced Series 900 and 900R multiuser and server standalone and rack-mount platforms.

The 197SP is a single-processor board that holds 128 Mbytes of programmable error-checking and correcting DRAM and 272 kbytes of cache memory (16 kbytes on the processor and 256 kbytes of secondary cache). The dual-processor 197DP holds a 50-MHz CPU, 128 Mbytes of DRAM, and 544 kbytes of cache memory (32 kbytes on-chip and 512 kbytes secondary).



Both models include SCSI-2 and Ethernet support and a mezzanine adapter to increase the DRAM capability to 512 Mbytes. The boards are built with a local-bus architecture that converts a local peripheral's 32-bit data bus to the MC88110's 64-bit system bus. They both run an enhanced version of Unix as well as a proprietary real-time operating system. The 197SP sells for $32,995, while the 197DP costs $44,995. Both boards are available now. A four-processor version of the board will be available early next year.

Motorola Computer Group, 2900 South Diablo Way, Tempe, AZ 85282; (408) 492-9090. CIRCLE 639

■ *RICHARD NASS*

MOTHERBOARDS ARE BUILT TO PCI SPEC

The PCI local bus can be used to accelerate the performance of PC subsystems, such as graphics. Three motherboards, the MEPent-AIO, SA486P-AIO, and SA486P-VIO, all conform to the PCI standard. All the boards contain a SCSI-2 host adapter and an IDE disk controller on the PCI bus for compatibility with most hard-disk drives. The MEPent-AIO is built with a 60- or 66-MHz Pentium processor. It contains three PCI slots and four EISA slots. The SA486P-AIO supports all Intel 486 and OverDrive processors, and has three PCI slots and four ISA slots. The SA486P-VIO is similar to the SA486P-AIO except that it is designed for use in a slim-line chassis. It also has a low-power mode that kicks in when the system is idle. All three PCI-based boards are available now. RN

Elitegroup Computer Systems Inc., 45225 Northport Ct., Fremont, CA 94538; (510) 226-7333. CIRCLE 640

VME BOARD SUITS EMBEDDED APPLICATIONS

The VME-based MVME162 now has a lower-priced sibling, the MVME162LX, which is suited for embedded applications. The LX holds up to 32 Mbytes of DRAM and 2 Mbytes of battery-backed SRAM, and is built with a 32-bit 25-MHz MC68LC040 microprocessor with 8 kbytes of internal cache memory. Two IndustryPack expansion ports allow for customization. The board contains front-panel I/O access and four serial ports. Software support is optional. The MVME162LX is offered in a VME or a busless configuration. Available now, prices start at $1095. RN

Motorola Computer Group, 2900 South Diablo Way, Tempe, AZ 85282. CIRCLE 645

68040-BASED SBC ELIMINATES BOTTLENECKS

Built with a 25-MHz 68040 microprocessor, the CPU-42 VMEbus single-board computer (SBC) breaks the three bottlenecks that tend to limit system performance—the system bus, the memory bus, and the I/O bus. This is accomplished using a VME64 system bus, a proprietary 144-bit memory bus,and 15-Mbyte/s I/O data throughput through two local expansion slots.

The board is suited for real-time applications that move large amounts of data at high speeds, such as imaging and simulation. It holds 16 Mbytes of DRAM, which communicates with the CPU over a 128-bit-wide bus (with 16 parity bits). As a result, the 68040 can perform entire cache-line transactions in one memory cycle. A cache-snoop capability maintains accuracy in the cache memory by comparing and updating data in the dual on-chip caches and main memory. Block- and multiplexed block-transfer cycles let the board read or write continuous data streams at 20 Mbytes/s.

Customized I/O is achieved using the two available mezzanine-board slots. The types of 32-bit modules that can be plugged in include Ethernet, SCSI, disk drives, and other types of serial I/O. Available now, the CPU-42 is priced at $4490 with 8 Mbytes of main memory in single units. RN

Force Computers Inc., 2001 Logic Dr., San Jose, CA 95124; (800) FORCE-99. CIRCLE 642

CARD INTEGRATES COLOR LCD INTO EMBEDDED SYSTEM

Designers can integrate color LCDs into their embedded systems using the Mini-LCD adapter. The adapter's small size and weight suits it for medical instrumentation and point-of-purchase units. It drives a Sharp LQ6-series 6-in. color LCD and includes an interface for a low-cost touch-screen input. The 4.4-by-3.8-in. card attaches directly to the back of the display and is driven by a Super VGA or CGA display controller module. Controlled by either hardware or software, the Mini-LCD can instantly switch between computer-generated and externally-sourced NTSC video signals.

The adapter includes a dc-to-dc converter to generate the –8 V dc required by the LCD, eliminating the need for a specialized power supply. A development kit is available that consists of the adapter, an LCD panel, a 4- by 4-in. touch-screen panel, interface cables, and driver software. With the exception of the touch-screen panel, all the components are assembled on a stand, ready to connect to the video source. In quantities of 100, the Mini-LCD sells for $140. The kit costs $3600. Both are available now.

***Ampro Computers Inc.**, 990 Almanor Ave., Sunnyvale, CA 94086; (408) 522-2100.* **CIRCLE 643**

■ *RICHARD NASS*

CONNECT HIGH-SPEED SCSI-2 PERIPHERALS TO THE VL-BUS

Connecting peripherals using a SCSI interface is one way of boosting their performance. To push the envelope even further, those same SCSI peripherals can be connected to a VL-Bus local bus using the AHA-2840VL host adapter.

The core of the board is an 8-MIPS RISC-based PhaseEngine processor that minimizes overhead by automating SCSI phase changes and advanced SCSI features. The proprietary chip is suited for multitasking and multithreaded SCSI operations. Instructions are downloaded to the PhaseEngine by the host CPU and a 64-byte scratch-pad memory stores the configuration information.

The 2840VL board is simple to install and configure. Running a BIOS-resident configuration utility, called SCSISelect, eliminates the need to set jumpers. It also detects the VL-Bus clock rate and sets itself accordingly. When new external peripherals are added to the system, the utility software lets the user reconfigure the system through software without opening the system. The board supports DOS and Microsoft Windows, with Windows NT support to come shortly.

***Adaptec Inc.**, 691 South Milpitas Blvd., Milpitas, CA 95035; (408) 945-8600.* **CIRCLE 644**

■ *RICHARD NASS*

CPU BOARD HOLDS UP TO FOUR 75-MHZ CHIPS

With advanced architectural features, including a distributed shared memory, a six-way crosspoint CPU-memory interconnect, and direct cache coherency, the Series 9000 multiprocessor board is designed with up to four 75-MHz R4400 RISC processors. Each processor has its own 1-Mbyte external cache memory, while the board holds a shared memory, up to 512 Mbytes. The 6U board is designed for real-time applications. Its crosspoint switch reduces bus loads and is faster than a traditional bus topology due to the shorter distances that signals have to travel. Available in the first quarter, prices start at $24,995. RN

Concurrent Computer Corp., 2 Crescent Pl., Oceanport, NJ 07757; (908) 870-4500. **CIRCLE 645**

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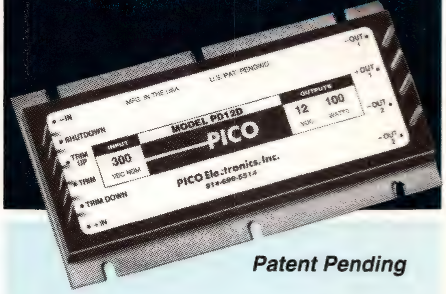

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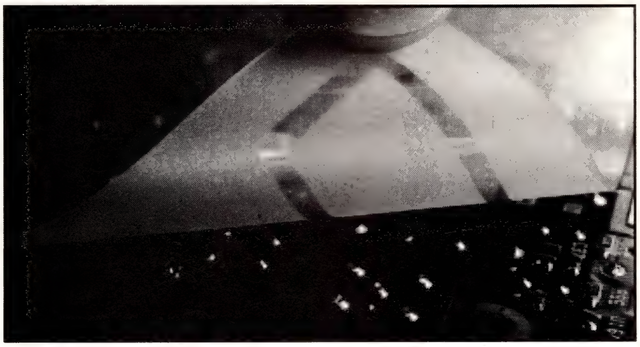
New PEEL'N SHIELD™ EMI gaskets lower installed cost!



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SMALL POWER MOSFETS REPLACE TWO TO-220S

A rated on-resistance of only 50 mΩ and continuous-current handling of 5 A is featured in the Little Foot Si9936DY dual power MOSFET. The device, aimed at applications in high-performance disk drives and high-end portable computers, is claimed as the first dual power MOSFET to offer this combination of current handling and low $R_{DS(on)}$ in a small-outline package. The Si9936DY MOSFET reduces heat generation and improves motor response in disk drives. Its 30-V rating allows it to handle the higher battery voltages typical of today's notebook computers. Used as a load switch, the device prolongs battery life by shutting down unneeded functions. It saves space by replacing two DPAKs or two TO-220 devices. Pricing in large OEM lots is $0.98. Samples and large production quantities are available immediately. DM

Siliconix, P.O. Box 54951, Santa Clara, CA 95056-0951; (800) 554-5565, ext. 94. **CIRCLE 646**

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A line of 28 single-, dual-, and triple-output linear ac-dc power supplies is intended for applications where tight regulation and low output noise are extremely critical. The HL family of supplies ranges in power from 15 to 90 W and operate from a user-selectable input of 100, 120, 220, 230, or 240 V ac. All carry UL, CSA, and TUV approvals and meet FCC Class B and VDE 0871 Class B conducted-EMI requirements for worldwide usage. Line and load regulation is ±0.5% for all models with output ripple of no more than 3 mV p-p. Remote-sense capability is standard on most models, and most outputs can be adjusted over a ±5% range. Prices range from $25 to $95 in OEM lots. Call for delivery information. DM

Computer Products Inc., 7 Elkins St., South Boston, MA 02127; Janice Williams, (617) 464-6656. **CIRCLE 647**

A Short Quiz for America's Executives

1. Would you like to help disadvantaged young people get an education—and a job? ☐ YES ☐ NO

2. Does your company have excess inventory, services or assets that could be used by colleges? ☐ YES ☐ NO

3. Could your company use an above cost tax deduction for qualified inventory donations? ☐ YES ☐ NO

If so, EAL's College Opportunity Program may be for you. EAL targets talented youngsters before they enter their freshman year of high school, then mentors them for four years until they graduate.

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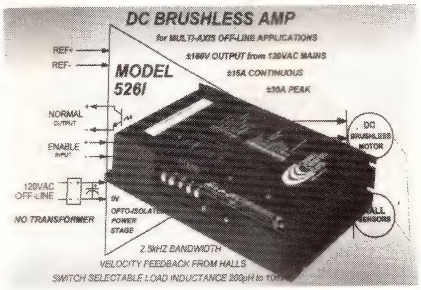
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Designed to drive brushless dc motors as large as 3.6 horsepower, the model 526I servoamplifier from Copley Controls features an isolated (floating) power stage. The isolation permits operation directly from a rectified 120-V ac line eliminating the need for bulky, 40-to-60 lbs., and expensive isolation transformers (or isolated dc power supplies). Only a full-wave bridge rectifier and a filter capacitor are needed between the ac line and the servoamplifier. Optical isolation links the "floating" dc power with the input control and feedback signals. Until now, servoamplifiers such as the 526I have required transformer-isolated dc power, which permits one side of the high-voltage source, and the feedback and input signals, to be referenced to ground.

No toy, the amplifier puts out ±15 A continuously and peak currents of ±30 while providing drive voltages between ±24 V and ±180 V. Efficiency at full load runs 95%. This switchmode (class D) amplifier operates at 25 kHz, giving it a bandwidth of 2.5 kHz and resulting in the excellent step response needed for applications requiring rapid acceleration and motor reversal.

Applications that can benefit from the 526I's power and bandwidth include motion-control systems that place emphasis on economy, power, and fast response. Multi-axis systems gain further economy by operating several amplifiers from a single, transformerless, high-voltage dc source. Typical examples range from numerically controlled machine tools to radar antennas.

The amplifier measures 8.5 in. by 5.5 in. by 2.25 in. and weighs 2.7 lbs. In lots of 1 to 9 it costs $625 each.

***Copley Controls Corp.**, 410 University Ave., Westwood, MA 02090; Jim Woodward, (617) 329-8200.* **CIRCLE 648**

■ *FRANK GOODENOUGH*

DRIVER RUNS OFF 1.8-V RAILS AND RULES THREE HIGH-SIDE MOSFETs

Turning on low-cost n-channel power MOSFETs connected as high-side switches requires pulling their gates 5 to 15 V above their drains. Power management in portable, battery-powered equipment represents a major application for the use of high-side-switch-connected power FETs and IGBTs, which switch power from a battery or supply to various subsystems within a laptop, notebook, or palmtop PC, or to perform similar functions in cellular phones or portable medical instrument. The LTC1163 triple high-side MOSFET driver meets these application needs. While running off a 1.8- to 6-V supply rail, it takes three separate digital input pulse trains and converts them to three output pulse trains of 6- to 12-V respectively. The chip can also drive low-side FET switches.

An internal charge pump develops the voltage, which is added to the supply rail. Moreover, designed to conserve battery power, the IC runs on a maximum standby current of a mere 1 μA. Typical operational current for each driver, when active, runs between 80 and 300 μA for supply voltages between 1.8 and 6. Rise and fall times of the output are controlled to prevent the emission of EMI and RFI. While operating from a 3.3 V rail and driving 1000 pF, it takes a maximum of 600 μs for the output of a channel to reach the supply voltage plus 2 V. Under similar conditions, turn off time to 0.5 V runs a maximum of 200 μs. With a 5-V supply rail, these times drop to 400 and 150 μs, respectively. In lots of 100, the CMOS LTC1163 costs $2.90 in an 8-pin SOIC package.

***Linear Technology Corp.**, 1630 McCarthy Blvd., Milpitas, CA 95035-7487; (800) 637-5545.*

CIRCLE 649

■ *FRANK GOODENOUGH*

THREE-PHASE MOTOR CONTROLLERS COME IN SMALL HYBRID PACKAGES

A rugged pair of three-phase motor controllers come in tiny hermetically sealed hybrid packages just 3.1 in. by 2.1 in. by 0.4 in. thick. Aimed at military, aerospace, and commercial avionics applications, the two controllers, the PWR-82500 and -82505 represent the first of a series of full-featured controllers. The PWR-82500 has MOSFET output stages rated at 100 V and 15 A. The PWR-82505 uses IGBTs protected by flyback diodes for its output stages, so it's rated at 500 V and 12 A.

Both devices are designed to employ external Hall-effect sensors for rotor-position feedback. They provide true four quadrant (both high-side and low-side switches are driven by pulse-width modulation) operation for six-step trapezoidal motor commutation. Each controller carries on-board analog control and pulse-width modulation circuits as well as digital commutation-control logic.

In quantities of 1 to 9, the PWR-82500 costs $999 each; the PWR-82505 costs $1049 each.

***ILC Data Device Corp.**, 105 Wilbur Pl., Bohemia, NY 11716; Mike Pitka, (516) 567-5600.*

CIRCLE 650

■ *FRANK GOODENOUGH*

OS UPDATE HAS MICROKERNEL ARCHITECTURE

Taking aim at hyper-embedded, hard real-time applications, version 3.0 of the Microware's OS-9 operating system has a preemptible kernel, faster interrupt response and context switching, and more efficient interprocess communication mechanisms. The OS upgrade also has improved determinism, enhanced memory-management facilities, and greater overall system call throughput.

For resource-limited embedded applications, Microware has the Atomic OS-9 runtime microkernel, 20% smaller and 15% faster than the standard v3.0 kernel, yet upwardly compatible. The microkernel has a subset of the functions in the OS-9 v.3 kernel, excluding development and debugging support, which aren't usually required in run-time environments.

Version 3.0 supports system-state preemption, which improves OS-9's determinism and interrupt response; as a result, kernel services can be preempted by higher priority tasks and interrupt handlers.

Microware to improve determinism has added system-state preemption to the operating system's core I/O file managers. It also has a new "buddy" memory allocator, assigning memory on a more predictable block size basis rather than on a "first fit" basis.

The v3.0 kernel's fast IRQ system call (F$FIRQ) in OS-9 and Atomic OS-9 cut the interrupt latency in half—to 3.0 µs—by performing a partial register save.

A developer's package consisting of the v3.0 kernel, Atomic kernel, IOMan I/O manager, and pipes, serial/parallel, disk, DOS disk, TCP/IP, and NFS is $4000 for Motorola 683xx processors, $5000 for Motorola 16-bit processors, and $6000 for Motorola 32-bit 680x0 processors. Target runtime licenses start at $50 a copy for Atomic OS-9 in hundreds.

***Microware**, 1900 N.W. 114th St., Des Moines, IA 50325; (515) 224-1929; fax -1352.* **CIRCLE 651**

■ *SHERRIE VAN TYLE*

EMBEDDED KERNEL ADDS FAULT TOLERANCE

The pSOS+m 2.0 multiprocessing kernel incorporates new facilities for fault tolerance, improved real-time performance, and flexible interprocessor communication. The kernel is aimed at telecommunications and process-control applications. pSOS+m 2.0, a multiprocessing variant of the pSOS+ embedded kernel, retains a small memory footprint (17 kbytes) and the ability to run pSOS+ applications in multiprocessing mode without modifying original program code.

The upgrade enables embedded application developers to create high-performance real-time, fault-tolerant systems and applications. pSOS+m applications now support various means of backing up and handing off processing loads in a multiprocessing system while maintaining system integrity. These include soft fail, in which applications can back up processes from a failing node to maintain system performance; hot swap, in which system operators can insert new nodes or processor boards into a running system without shutting down; and rejoin, which allows replacement of failing boards with new ones.

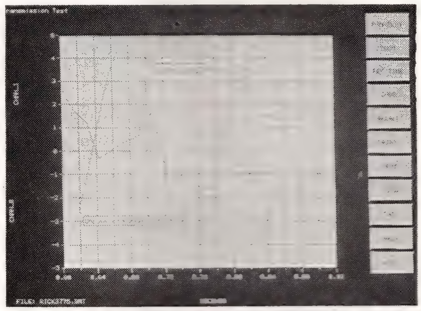
Overall, pSOS+m 2.0 runs 30 to 50% faster than the earlier version. The addition of asynchronous interprocessor communication services and variable length message queues improves performance of high-reliability multiprocessing systems compared to those using synchronous communications because the message-sending kernel can go on to other business before receiving an acknowledgment from the message-receiving note. Variable-length message queues add programming flexibility and processor utilization efficiency. pSOS+m 2.0 supports Motorola 68000 series and Intel i960 processors. First-copy development packages begin at $6000, with production licenses incorporating quantity discounts.

***Integration Systems Inc.**, 3260 Jay St., Santa Clara, CA 95054-3309; (408) 980-1500; fax -0400.* **CIRCLE 652**

■ *SHERRIE VAN TYLE*

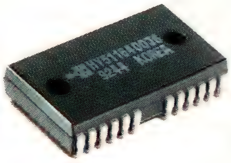
ANALYZER SOFTWARE SUPPORTS 80 CHANNELS

Enhanced to record up to 80 channels concurrently at 100 kHz to disk and 1 MHz to memory, ChartStream Recorder/Analyzer software version 2.0 is aimed at high-speed, multichannel data recording and analysis. Typical applications include process monitoring, data logging, post-process analysis, and trend analysis. All available hardware gains are supported, up to a gain of 200. As before, when data is recorded to disk, it can also be displayed in real-time strip-chart, scatter, or X-Y plots. Version 2.0 can display up to 10 real-time pages and now has pan and zoom capabilities. Also new is waveform playback, which enables a user to zoom in on a displayed waveform and review the data on screen. When an event of interest is found, a mouse click stops the playback at the event. When combined with one of the company's data-acquisition boards and a PC, ChartStream becomes a full-fledged data acquisition, analysis, and display system. The program lists for $595; upgrades, $150. SVT



Intelligent Instrumentation, a Burr-Brown Co., 6550 S. Bay Colony Dr., MS 130, Tucson, AZ 85706; (602)573-0887;fax-0522. **CIRCLE 653**

WITH HYUNDAI'S 16M DRAM



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	HY5117400/L	2K Cycle/32ms	
	HY5116410/L(*)	4K Cycle/64ms	
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CIRCLE 124 FOR U.S. RESPONSE

CIRCLE 125 FOR RESPONSE OUTSIDE THE U.S.

NETWORK FAX SERVER GETS UPGRADE

Version 2.1 of Object-Fax network fax server software sends faxes in a fraction of the time taken by the previous version. It offers DOS support and the ability to route incoming faxes through MAPI and VIM-based e-mail systems. Other new features include an option to automatically print all incoming and outgoing faxes and to have the server print transmission reports for them. It also supplies a dynamic data exchange (DDE) link that makes it possible to fax-enable Windows applications. Pricing is per fax server and by number of users; one fax server with a five-user license lists for $990. SVT

Traffic Software Inc., 360 W. 31st St., New York, NY 10001-2793; (212) 714-1584; -1691. **CIRCLE 654**

MIDDLEWARE TOOL EASES HOST LINKS

A middleware application development tool enables developers to create PC host communication-related applications using Microsoft's Visual Basic programming. QuickApp for Windows, when used with DCA's IRMA Workstation for Windows 2.1.2 or newer (IWW), is point-and-click software that insulates developers from the complexities of high-level application program interfaces. As a result, developers can create end-user applications using a two-phase approach without having expert knowledge of IBM communication software.

In the first phase a developer create a PC front-end to a mainframe application launches a QuickApp for Windows with IWW. Then s/he logs on to the mainframe and starts the application program to operate it while QuickApp captures each screen into its files and monitors the keystrokes and records the sequence of events. The developer can sign off the mainframe and complete the PC front-end application using the capture screens and its associated logic that reside in the QuickApp record file without tying up costly host resources. During the second phase, developers use Microsoft Visual Basic and QuickApp's record file and custom controls to assist in generating all the necessary code, commands, forms, objects, and event codes creating the final application. List price is $295. SVT

Digital Communications Associates Inc., 1000 Alderman Dr., Alpharetta, GA 30202-4199; (800) 348-3221; fax (404) 442-4364. **CIRCLE 655**

RENDERING PORTED TO SILICON GRAPHICS

Version 5.0 of Conceptual Design & Rendering Software (CDRS) now runs on workstations from Silicon Graphics. With CDRS, designers can create and modify free-form surface models. The design is captured in an electronic format that can be sent to engineering systems for analysis or to manufacturing machines for milling. Software prices range from $18,000 to $100,000, depending on options and configurations. SVT

Evans & Sutherland Design Software Group, 580 Arapeen Dr., Salt Lake City, Utah 84108; (801) 582-5847; fax -9413. **CIRCLE 656**

CASE TOOLS TARGET CLIENT/SERVER

With the Information Engineering Facility (IEF) for Client/Server, developers can generate complete client/server applications across multiple platforms. IEF for Client Server is part of the company's framework for enterprise engineering, encompassing products and services for business-process reengineering, application development, middleware, and transition engineering of legacy systems. The facility offers model-driven development, support of multiple client/server application styles, reduced effort to reflect change, and a wide range of platforms. List prices begin at $11,000, with introductory-package pricing and quantity-discount programs available. SVT

Texas Instruments Inc., 6670 Chase Oaks Blvd., Plano, TX 75023; (800) 336-5236. **CIRCLE 657**

DEBUGGER WORKS WITH HMI SYSTEMS

SourceGate II, a source-level debugger for the HMI development systems product line, supplies emulator control and source-level debugging for C and Ada compilers under IBM PC, Hewlett-Packard, and Sun-based platforms with native GUI environment support for Windows, Windows, NT, Unix, W Windows/Motif, and X Windows/Open Look. The package integrates source-level debugging with emulator control functions within the Windows interface. After executable target code is downloaded, commands to start, stop, and single-step may be issued. Throughout debugging, system status is reported while registers and other system parameters may be monitored in user-selectable windows. SourceGate II software for IBM PC-based host systems is included with each of HMI's 200 series emulators, LITE series emulators, background mode debuggers, and CPU simulators. Contact the company for pricing information. SVT

Huntsville Microsystems Inc., P. O. Box 12415, Huntsville, AL 35815; (205) 881-6005; fax 882-6701. **CIRCLE 658**

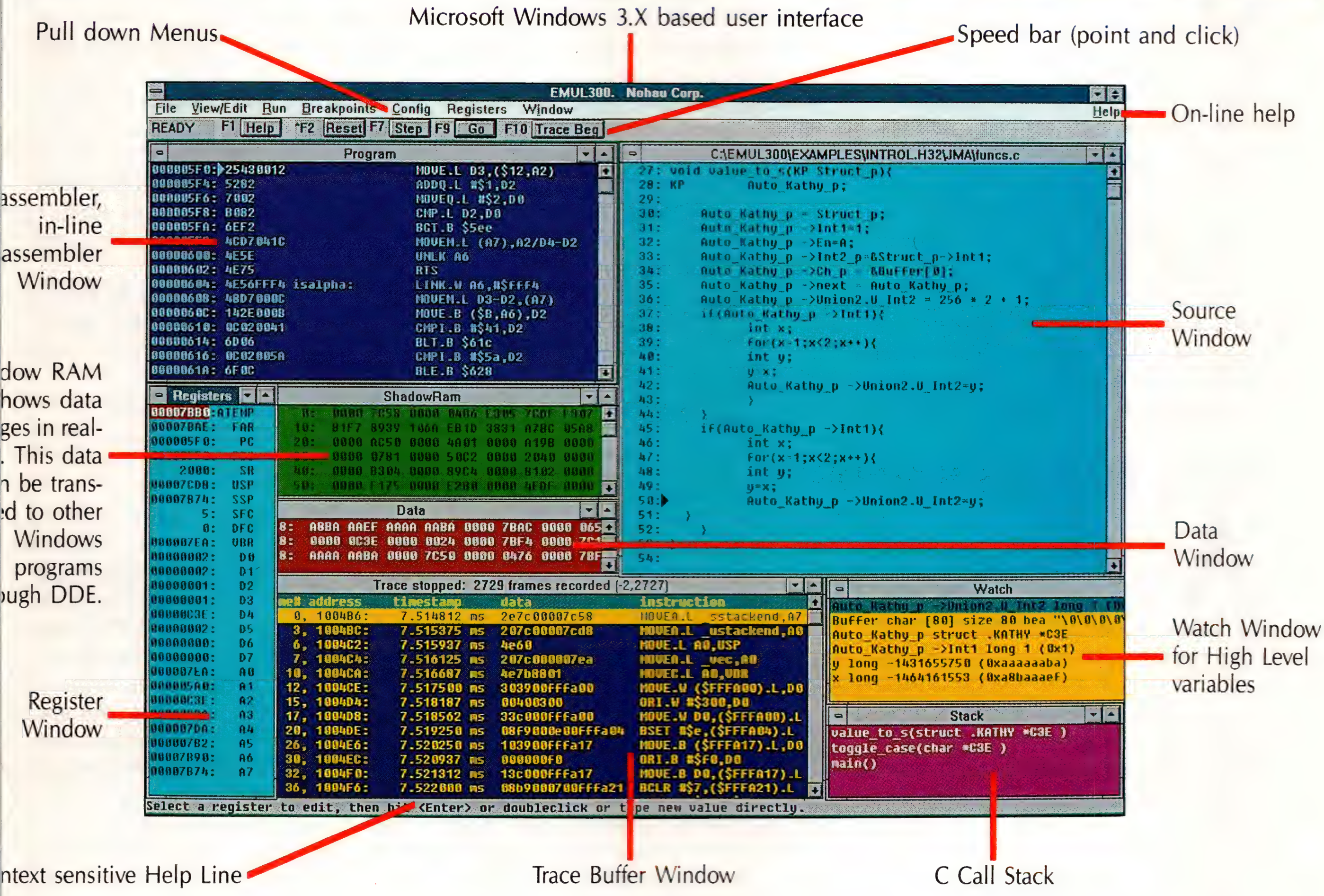
TOOLS SUPPORT DEBUGGING DSP BOARDS

A debugging tool for Texas Instruments' TMS320C40 digital signal processors enables a design team on a network to develop and debug software running on one or more multichip boards at once in a VME card cage. The Multiuser/multiboard DSP debugger from Mizar debugs C source code; Ada capabilities can be added as an option. If the boards in a system have multiple DSP chips on them, the debugger enables developers to isolate individual chips and debug software in a separate window on their Sun, Hewlett-Packard, or other workstations under X Windows on a network. A single-user license is $3995. SVT

Mizar Inc., 2410 Luna Rd., Carrollton, TX 75006; (214) 247-8849; fax 277-4666. **CIRCLE 659**

In-Circuit Emulators and Background Debuggers

68300 68HC16



```
000005F0:▶25430012                MOVE.L D3,($12,A2)
000005F4: 5282                    ADDQ.L #$1,D2
000005F6: 7002                    MOVEQ.L #$2,D0
000005F8: B082                    CMP.L D2,D0
000005FA: 6EF2                    BGT.B $5ee
          4CD7041C                MOVEM.L (A7),A2/D4-D2
00000600: 4E5E                    UNLK A6
00000602: 4E75                    RTS
00000604: 4E56FFF4 isalpha:       LINK.W A6,#$FFF4
00000608: 48D7000C                MOVEM.L D3-D2,(A7)
0000060C: 142E000B                MOVE.B ($B,A6),D2
00000610: 0C020041                CMPI.B #$41,D2
00000614: 6D06                    BLT.B $61c
00000616: 0C02005A                CMPI.B #$5a,D2
0000061A: 6F0C                    BLE.B $628
```

```
void value_to_s(KP Struct_p){
KP          Auto_Kathy_p;

    Auto_Kathy_p = Struct_p;
    Auto_Kathy_p ->Int1=1;
    Auto_Kathy_p ->En=A;
    Auto_Kathy_p ->Int2_p=&Struct_p->Int1;
    Auto_Kathy_p ->Ch_p = &Buffer[0];
    Auto_Kathy_p ->next = Auto_Kathy_p;
    Auto_Kathy_p ->Union2.U_Int2 = 256 * 2 + 1;
    if(Auto_Kathy_p ->Int1){
          int x;
          for(x=1;x<2;x++){
          int y;
          y=x;
          Auto_Kathy_p ->Union2.U_Int2=y;
          }
    }
    if(Auto_Kathy_p ->Int1){
          int x;
          for(x=1;x<2;x++){
          int y;
          y=x;
          Auto_Kathy_p ->Union2.U_Int2=y;
  }
    }
```

```
00007BB0:ATEMP
00007BAE:  FAR
000005F0:   PC
    2000:   SR
00007CD8:  USP
00007B74:  SSP
       5:  SFC
       0:  DFC
000007EA:  VBR
00000002:   D0
00000002:   D1
00000001:   D2
00000001:   D3
00000C3E:   D4
00000002:   D5
00000000:   D6
00000000:   D7
00007EA:    A0
000005A0:   A1
00000C3E:   A2
            A3
000007DA:   A4
000007B2:   A5
00007B90:   A6
00007B74:   A7
```

```
 0:  0000 7C58 0000 0A06 E305 7CDF F907
10:  B1F7 8939 106A EB1D 3831 A78C 05A8
20:  0000 AC50 0000 4A01 0000 A19B 0000
     0000 0781 0000 50C2 0000 2040 0000
40:  0000 B304 0000 89C4 0000 8102 0000
50:  0000 F175 0000 E280 0000 4FDF 0000
```

```
8:  ABBA AAEF AAAA AABA 0000 7BAC 0000 065
8:  0000 0C3E 0000 0024 0000 7BF4 0000 7C1
8:  AAAA AABA 0000 7C50 0000 0476 0000 7BF
```

```
Trace stopped:  2729 frames recorded (-2,2727)
me# address   timestamp     data              instruction
 0, 1004B6:   7.514812 ms   2e7c00007c58      MOVEA.L  sstackend,A7
 3, 1004BC:   7.515375 ms   207c00007cd8      MOVEA.L  _ustackend,A0
 6, 1004C2:   7.515937 ms   4e60              MOVE.L A0,USP
 7, 1004C4:   7.516125 ms   207c000007ea      MOVEA.L  _vec,A0
10, 1004CA:   7.516687 ms   4e7b0801          MOVEC.L A0,VBR
12, 1004CE:   7.517500 ms   303900FFFa00      MOVE.W ($FFFA00).L,D0
15, 1004D4:   7.518187 ms   00400300          ORI.W #$300,D0
17, 1004D8:   7.518562 ms   33c000FFFa00      MOVE.W D0,($FFFA00).L
20, 1004DE:   7.519250 ms   08F9000e00FFFa04  BSET #$e,($FFFA04).L
26, 1004E6:   7.520250 ms   103900FFFa17      MOVE.B ($FFFA17).L,D0
30, 1004EC:   7.520937 ms   000000F0          ORI.B #$F0,D0
32, 1004F0:   7.521312 ms   13c000FFFa17      MOVE.B D0,($FFFA17).L
36, 1004F6:   7.522000 ms   08b9000700FFFa21  BCLR #$7,($FFFA21).L
```

```
Auto_Kathy_p ->Union2.U_Int2 long 1 (0x
Buffer char [80] size 80 bea "\0\0\0\0
Auto_Kathy_p struct .KATHY *C3E
Auto_Kathy_p ->Int1 long 1 (0x1)
y long -1431655750 (0xaaaaaaba)
x long -1464161553 (0xa8baaaef)
```

```
value_to_s(struct .KATHY *C3E )
toggle_case(char *C3E )
main()
```

```
Select a register to edit, then hit <Enter> or doubleclick or type new value directly.
```

EATURES

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CIRCLE 242 FOR U.S. RESPONSE

CIRCLE 243 FOR RESPONSE OUTSIDE THE U.S.

TOOLS COMBINE NUMERIC, SYMBOLIC COMPUTATION

Speed, accuracy, and reliability are promised in an environment for integrated numeric and symbolic computation. Extensions to MATLAB, the Symbolic Math Toolbox and the Extended Math Toolbox from The MathWorks integrate symbolic computing with high-performance numeric computation. Both products are based on embedded versions of Maple V, developed by Waterloo Maple Software.

The toolbox includes new MATLAB commands for 50 of the most commonly used symbolic functions in Maple. The toolbox also supplies commands for variable precision arithmetic, direct access to the Maple kernel and Maple's core math library and linear algebra module, which come with the product.

The extended toolbox is a superset that includes access to Maple's programming language, the ability to create and execute Maple functions and applications, and the complete set of more than 20 Maple software packages for specialized fields such as number theory, power series, and geometry. MATLAB toolboxes extended the product by adding specialized functions for particular applications. These include neural networks, signal processing, control system design and analysis, system identification, and optimization.

Pricing for the Symbolic Math Toolbox is $495 and the Extended Math Toolbox is $695. University discount pricing for the symbolic toolbox is $195; the extended product, $495. The first platforms are the Sun Sparcstation and Windows 3.1. Versions for the Macintosh, HP 700 series, Silicon Graphics, IBM RS/6000, DECstation Ultrix, Alpha OSF/1, and VAX/VMS are expected later this year.

***The MathWorks Inc.**, 24 Prime Park Way, Natick, MA 01760; (508) 653-1415; fax (508) 653-2997.* **CIRCLE 660**

■ *SHERRIE VAN TYLE*

REAL-TIME OS BUILDS ON UNIX SYSTEM V, R 4.2

A real-time operating system for Intel platforms, based on Unix System V Release 4.2, affords System V functionality for developing real-time systems for acquisition and control applications. Based on Unix System V source code, Venix retains compatibility while gaining the deterministic qualities of a true-real-time OS, its maker points out.

Venix 4.2.1 has a preemptable kernel to ensure responsiveness to external devices that need servicing. To further slash response times, Venix uses a contiguous file structure that eliminates fragmented and scattered files that consume access time. Also, a task can be locked into memory so that no time is lost retrieving it from disk. Bounded context switch latencies guarantee response times. Fixed priority scheduling ensures that the highest priority runable process controls the CPU.

The Venix system comes with TCP/IP, NFS, W Windows, Motif, and OpenLook. Also supported are USL-supplied W Windows and Motif along with W Windows release 5 and Motif 1.2.2 for added capability and portability. The OS runs on 386, 486, and Pentium PCs with 6 Mbytes of memory, a 100-Mbyte disk, and a 6150 cartridge tap. The toolkit allows the Venix kernel to be made embeddable or ROMable for users and for resale by OEMs. Run-time licenses are priced accordingly. The kernel is $59 for quantities of 2000. The Workstation system, which includes the real-time OS, NFS, and TCP/IP networking, W-Windows, OpenLook, and Motif graphical user interfaces, and the Veritas journaling file system, is $995. The development system, which adds to the foregoing an ANSI C compiler library of real-time functions, GUI development software, real-time development utilities, and I/O device drivers and sources, is $2395 per seat.

***VentureCom**, 215 First St., Cambridge, MA 02141; (617) 661-1230.* **CIRCLE 661**

■ *SHERRIE VAN TYLE*

VIDEO-CARD TOOLS DELIVER HIGH-END SOLUTIONS

System designers interested in quickly developing Microsoft Windows-compatible video add-in cards that feature 30 frames/s video capture and playback, full audio capability and up to 1280-by-1024-pixel resolution will get lots of help from a new developer's kit.

Since the kit implements Brooktree Corp.'s VideoCache architecture, the designs are based on the company's Bt885 Video CacheDAC and its Bt812 video decoder chips. The architecture reduces component and memory costs for high-end systems by eliminating the need for separate graphics and video subsystems. In addition to sample hardware, schematics and software drivers, the kit implements the software codecs supported by Microsoft's Video for Windows such as Intel's Indeo and Media Vision's MoTive.

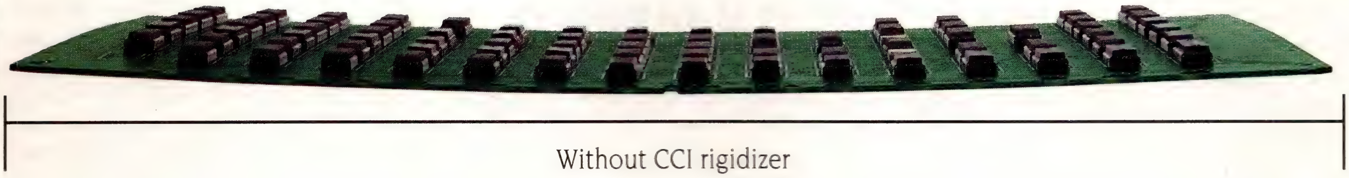
Two add-in card designs are included. The first integrates the Bt812 decoder, a video controller, and 0.25 Mbytes of RAM. It is for high-bandwidth VESA Advanced Feature Connector (VAFC) systems and assumes the host system already has a Bt885 CacheDAC on the motherboard or on a graphics card.

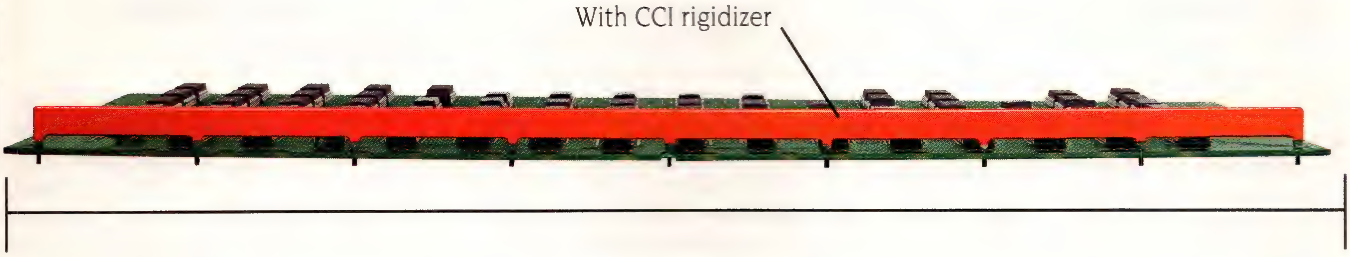
The second design is for a complete video capture and GUI accelerator solution. It integrates the Bt885 into the first design to mix the video and audio streams. Designers can also develop a graphics daughtercard to interface with this design that can carry a complete graphics subsystem supporting 1280-by-1024-pixel resolution. The kit is available now priced at $1800.

***Brooktree Corp.**, 9950 Barnes Canyon Rd., San Diego, CA 92121; (619) 452-7580.* **CIRCLE 662**

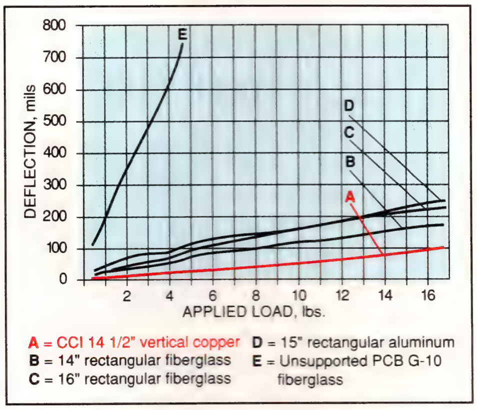
■ *JACK SHANDLE*

Boards stiffened with CCI rigidizers fit better and perform better.





Warped boards mean trouble. They won't fit correctly into the slot or rack, and you can expect cracks in soldering and connections. CCI rigidizers solve your warpage problems quickly and economically in both high and low current applications. They can carry up to 64 AMPS and can be used as shields for noise-sensitive electronic components, as well as mechanical vibration shock absorbers. They'll even protect the PCB from cracks on solder joints and PCB traces. And the one-step installation requires no hardware. Send for a free applications bulletin to learn more.



A comparison showing significantly better performance with CCI board stiffeners than with other conventional methods.

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CIRCLE 257 FOR U.S. RESPONSE **CIRCLE 258 FOR RESPONSE OUTSIDE THE U.S.**

REFERENCE MANUAL HAS APP NOTES

Engineers working on analog, mixed-signal, or DSP designs may find helpful a 1344-page collection of technical articles, application notes, tutorials, and design ideas from Analog Devices, Norwood, MA. Material is reprinted from trade press articles and company application notes; topics range from the basics of noise and grounding to advanced topics such as multichannel systems. The 1993 Applications Reference Manual is $9.95. Contact (617) 937-1428; fax (617) 821-4273. SVT **CIRCLE 900**

BOOKLETS OFFER MEASUREMENT TIPS

Three booklets from Keithley Instruments' Test Instrumentation Group, Cleveland, Ohio, offer a series of application notes that describe how to simplify test configurations, improve throughput, and cut costs. The "General Measurements" booklet covers subjects ranging from locating short circuits on pc-boards to measuring power-line harmonics. "Semiconductor Measurement" covers zener diode characterization, parametric testing of packaged semiconductors, and other topics. Subjects in "Low-Level Measurement" include sources of errors when measuring high resistances, how to use a cryogenic liquid level sensor, and measuring the resistance of insulating materials. JN **CIRCLE 901**

SOCKETS AND ADAPTERS SOLVE BOARD REDESIGNS

A catalog from Aries Electronics, Frenchtown, N.J., features its Correct-A-Chip interconnection and packaging products, which offer cost-effective solutions to board upgrade or rework problems without redesigns. The six-page catalog provides an introduction to the technology. Included is the Correct-A-Chip socket, a device that reroutes the circuit paths and pinouts from the original design to meet the needs of the new design. The catalog also covers the adapter, which converts from one termination style to another. A problem-and-solution section hints at the variety of difficulties the technology can solve. DM **CIRCLE 902**

FULL-LINE CATALOG COVERS 40,000 PRODUCTS

The No. 930 full-line catalog from Molex Inc., Lisle, Ill., features more than 40,000 products with descriptions, photos, drawings, specifications, and ordering information. Products include micro- and nano-miniature connectors, ribbon-cable systems, switches, pc-board connectors, edge-card connectors, FFC connectors, sockets, pin-and-socket connectors, application tooling, solderless terminals, environmental connectors, and I/O connectors. Also included is a complete worldwide directory of Molex distributors and representatives. DM **CIRCLE 903**

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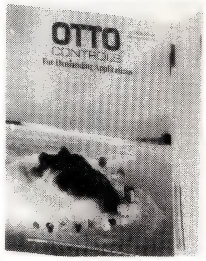

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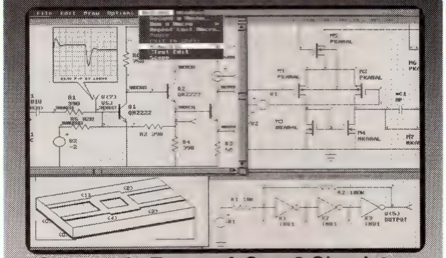

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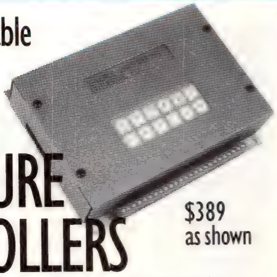

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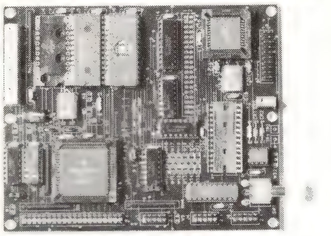

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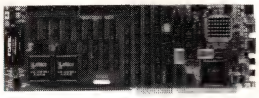

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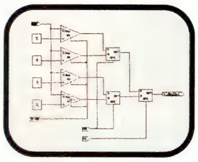

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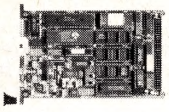

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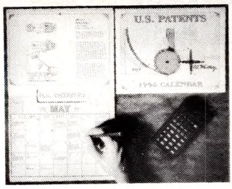

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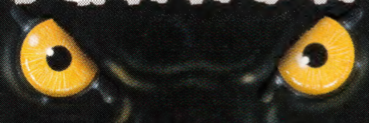

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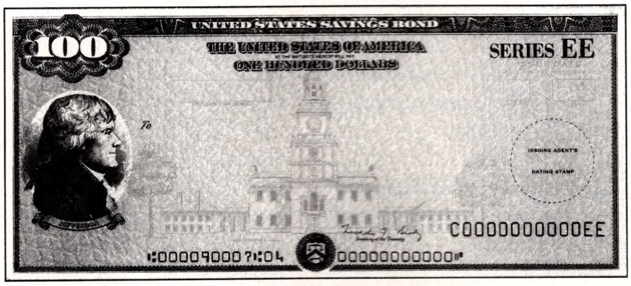
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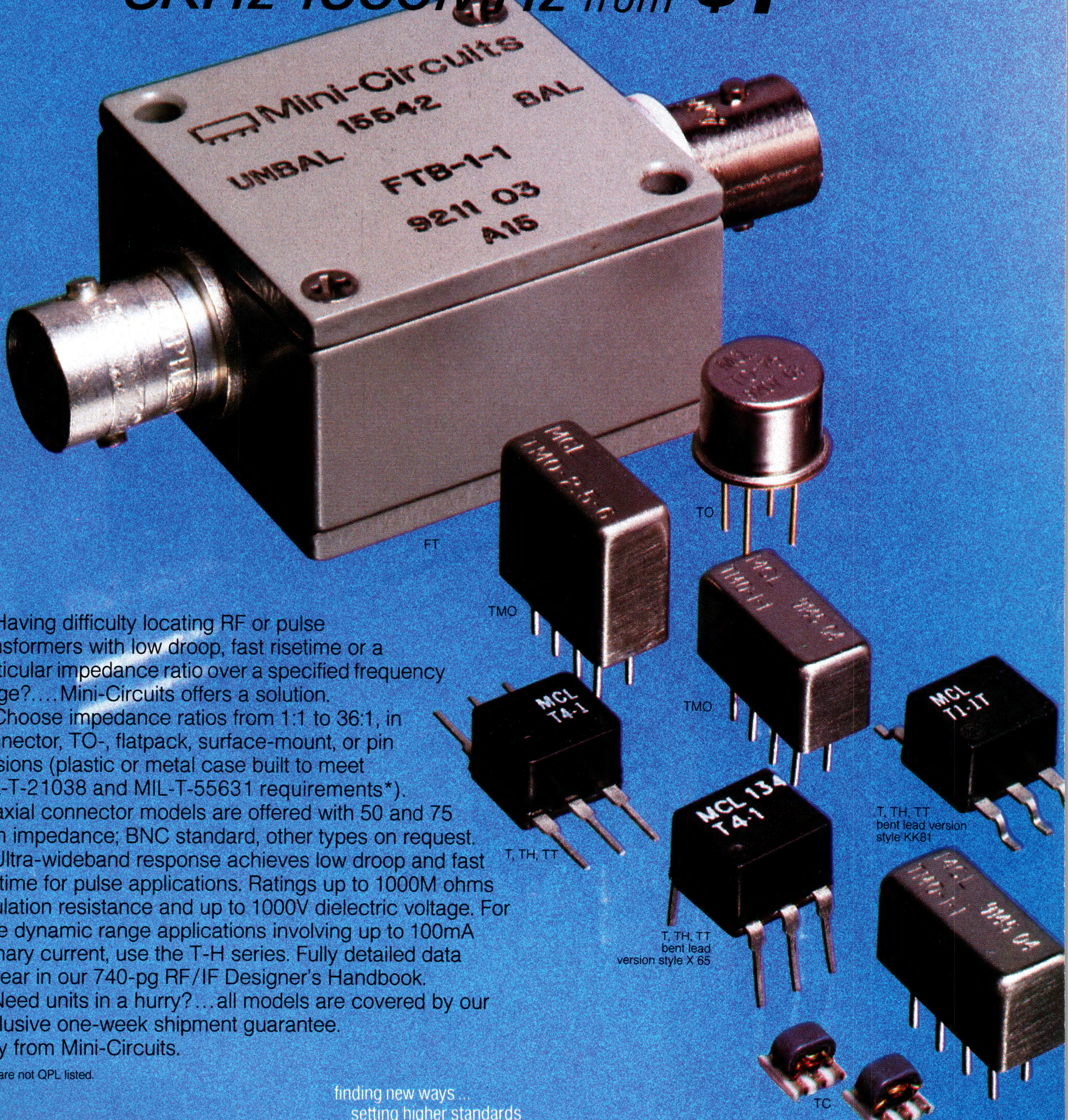

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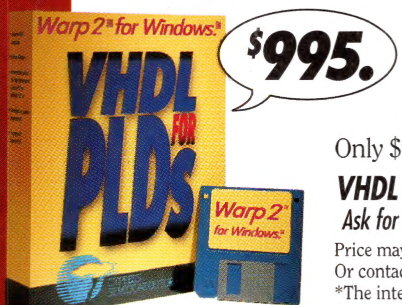

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